XVME-531
6U 16-Channel Analog Output Module

USER'S MANUAL

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1.1 INTRODUCTION

The XVME-531 is a powerful VMEbus compatible analog output module that is capable of performing digital to analog conversions with 12 bit resolution. The module has the capability of updating multiple D/A channels simultaniously. The XVME-531 analog output module is available in two versions:

- XVME-531/1, providing 16 voltage output channels (either unipolar or bipolar) in the ranges 0-10 V, ±5 V or ±10 V.
- XVME-531/2, providing 16 isolated (500 V) channels which may be configured for either voltage output (in the same ranges as the above option) or current loop output (4 to 20 mA).

1.2 CHAPTER/APPENDIX DESCRIPTION

The chapters in this manual are organized as follows:

Chapter One: A general description of the XVME-531 Analog Output Module, including functional and environmental specifications, a block diagram, and VMEbus compliance information.

Chapter Two: Module installation information including system requirements, jumpers, switches and connector pinouts.

Chapter Three: Information required to program the module for analog output operation.

Chapter Four: Procedures for analog output calibration.

Appendix A: Xycom Standard I/O Architecture: background information describing the standard I/O hardware relevant to the XVME-531.

Appendix B: VMEbus Connector/Pin Description: listings of the VMEbus signals, connectors, and pin numbers.

Appendix C: Quick Reference Guide (blue pages): compact reference of tables containing information on jumpers, switches, LEDs, etc.

Appendix D: Diagrams and Schematics: module assembly drawing, block diagram, and schematics.

1.3 MODULE OPERATIONAL DESCRIPTION

The XVME-531 module consists of the following parts:

- VMEbus interface circuitry
- Xycom standard I/O module circuitry
- D/A conversion circuitry

Figure 1-1 shows the operational block diagram of the XVME-531 Analog Output Module.

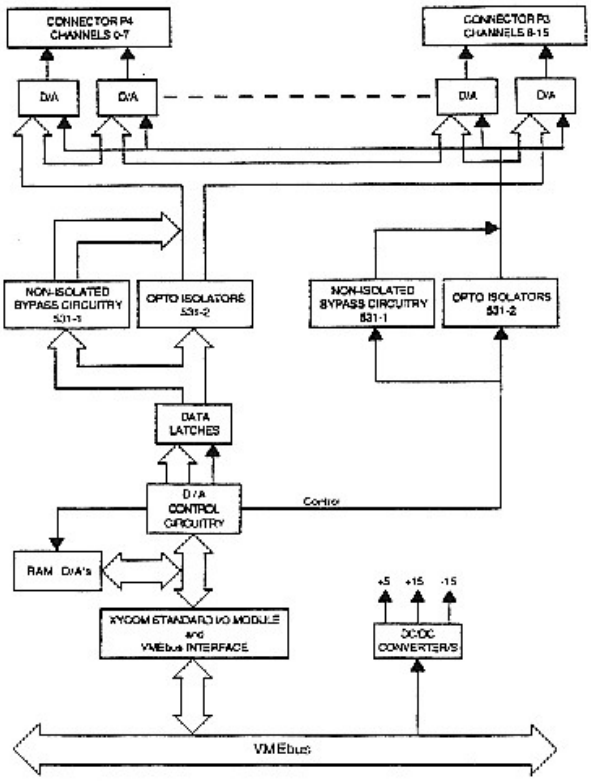


Figure 1-1. XVME-531 Block Diagram

1.3.1 **VMEbus Interface Circuitry**

The VMEbus interface circuitry provides all the necessary circuitry to receive and generate the signals required by the VMEbus specification for a 16 bit slave.

1.3.2 **Xycom Standard I/O Module Circuitry**

The XVME-531, like all Xycom XVME I/O modules, conforms to the Xycom Standard I/O Architecture. This architecture is intended to make the programming of Xycom VMEbus I/O modules simple and consistent. The following features apply to the operation of this module.

Module Address

Space - The XVME-531, and all XVME I/O modules are controlled by writing to addresses within the 64 Kbyte Short I/O address space or the upper 64 Kbytes of the standard address space. A module can be configured to occupy any of the 64 available 1 Kbyte blocks within each of these address spaces. The 1 Kbyte block occupied by the module is called the I/O interface block and contains all the module's programming registers, module identification data, and I/O registers. Within the I/O interface block, the address offsets are standardized across the XVME product line, so registers and data are at one location.

Module I.D. - The module has I.D. information which provides its name, model number, manufacturer, and revision level at a location consistent with other Xycom modules.

Status/Control Register - This register is always located at module base address +81H. The lower two bits (red and green LED bits) are standard from module to module.

Appendix A provides more detailed information about Xycom's Standard I/O Architecture.

1.3.3 **Digital to Analog Conversion Circuitry**

The digital to analog conversion circuitry contains the following features:

- D/A channel control circuitry controls all modes and operations of D/A convertors
- Opto-Isolators used to isolate **between** the VMEbus and the analog section on the XVME-531/2
- Non-Isolated bypass circuitry used on the XVME-531/1
- Data latches used to store data to be converted to analog
- 12-bit D/A convertors
- RAM D/A's used to read D/A channel latches

1.4 SPECIFICATIONS

Table 1-1. XVME-531 Specifications

Characteristic	Specification
Number of Channels	16
Optical Isolation	500 Volts
Voltage Output	
Resolution	12 Bits
Accuracy	
**Overall Error	±.5 LSB, ± .0122%
Monotonicity	Guaranteed
Settling Time (to .012%)	
10 V Range (0 10 V, ±5 V)	5 usec.
20 V Range (±10 V)	6 usec.
Offset T.C. (Bipolar Mode)	10 ppm/C max
Offset T.C. (Unipolar Mode)	10 ppm/C max
Gain T.C.	20 ppm/C max
Current Output Characteristics (531/2 only)	
Resolution	12 Bits
Compliance Voltage	10.5 Volts @20mA
Accuracy	
**Overall Error	±.66 LSB, ±.016%
Settling Time (to 1/2 LSB)	80 usec.
Load Resistance Range	50 to 525 Ohms
Offset T. C.	30 ppm/C max
Gain T. C.	50 ppm/C max
*Conversion Time	
XVME-531/1	400 nsec. typ.
XVME-531/2	4.7 usec. typ.
Supply Voltage	
Supply Current	
XVME-531/1	1.8 A typ. with outputs at full scale
XVME-531/2	3.2 A typ. with outputs at full scale (4-20 mA mode)

Conversion Time is defined as the time required to start a conversion. It is measured from the start of DS0 to when the analog output first starts to change.

**Overall Error is specified with gain and offset trimmed and is defined as the deviation from a straight line passing through the end points of the range. It is expressed in terms of bits and in terms of deviation as a percent of the full scale range (i.e., ±.5 LSB is ±.0122% FSR)

Table 1-1. XVME-531 Specifications (Continued)

Characteristic	Specification
Environmental	
Temperature	
Operating	0º to 65º C (32º to 149º F)
Non-operating	-40º to 85º C (-40º to 185º F)
Humidity	
Operating	5 to 95% RH non-condensing
Shock	
Operating	30 g peak. 11 msec
Non-operating	50 g peak. 11 msec
Vibration	
Operating	5 to 2000 Hz .015" peak-to-peak displacement 2.5 g (maximum) acceleration
Non-operating	5 to 2000 Hz .030" peak-to-peak displacement 5.0 g (maximum) acceleration
Board Dimensions	Form factor: Double (160 mm x 220 mm)
VMEbus Compliance	
Fully compatible with VMEbus standard IEEE 1014 A24/A16:D16 DTB Slave AM Codes 29,2D,39,3D response (STAT)	

2.1 INTRODUCTION

This chapter provides the information needed to configure and install the XVME-531 Module.

2.2 SYSTEM REQUIREMENTS

The XVME-531 Analog Output Module is a double-high (6U) VMEbus-compatible module. To operate, it must be properly installed in a VMEbus backplane. The minimum system requirements for operation of the module are one of the following:

a. A host processor installed in the same backplane

and

A properly installed controller subsystem.

or

b. A host processor module which incorporates and on-board controller subsystem.

2.3 LOCATION OF JUMPERS AND SWITCHES RELEVANT TO INSTALLATION

Prior to installing the Analog Output Module, it will be necessary to configure several jumper/switch options. The configuration of the jumpers/switch is dependent upon which of the module operational capabilities are required for a given application. The jumper/switch options can be divided into two categories:

- VMEbus-related options
- Digital to analog conversion options

Figure 2-1, on the following page, shows the location of the jumpers and switches on the XVME-531 Module.

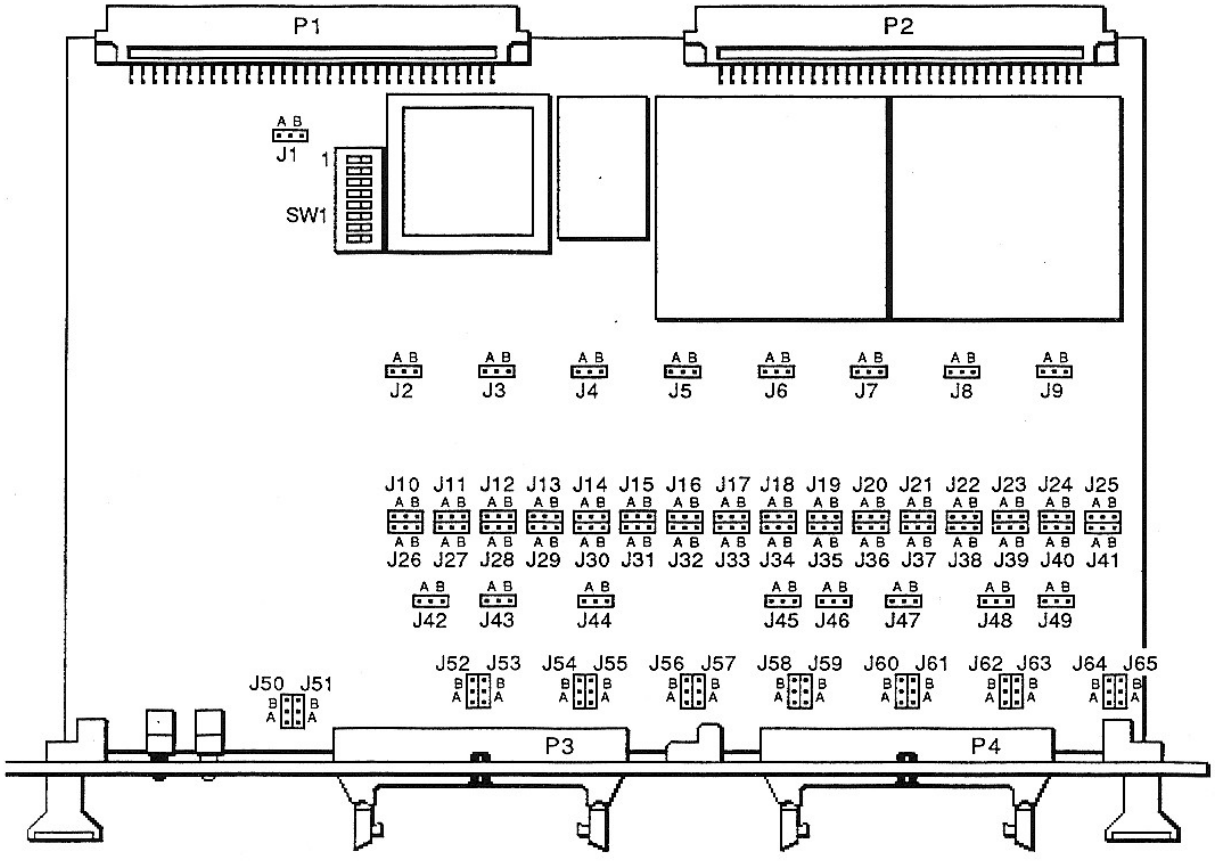


Figure 2-1. XVME-531 Jumper and Switch Locations

2.4 **JUMPERS**

The jumpers used on the XVME-531 are listed in Table 2-1 below. Sections 2.5 through 2.6 discuss the jumpers and switches in more detail.

Table 2-1. Jumper Listing

Jumper	Function
J1	SYSFAIL jumper
J2	Selects straight/offset binary or two's compliment for channel 14
J3	Selects straight/offset binary or two's compliment for channel 12
J4	Selects straight/offset binary or two's compliment for channel 10
J5	Selects straight/offset binary or two's compliment for channel 8
J6	Selects straight/offset binary or two's compliment for channel 6
J7	Selects straight/offset binary or two's compliment for channel 4
J8	Selects straight/offset binary or two's compliment for channel 2
J9	Selects straight/offset binary or two's compliment for channel 0
J10	Used to select Unipolar or Bipolar operation for channel 15
J11	Used to select Unipolar or Bipolar operation for channel 14
J12	Used to select Unipolar or Bipolar operation for channel 13
J13	Used to select Unipolar or Bipolar operation for channel 12
J14	Used to select Unipolar or Bipolar operation for channel 11
J15	Used to select Unipolar or Bipolar operation for channel 10
J16	Used to select Unipolar or Bipolar operation for channel 9
J17	Used to select Unipolar or Bipolar operation for channel 8
J18	Used to select Unipolar or Bipolar operation for channel 7
J19	Used to select Unipolar or Bipolar operation for channel 6
J20	Used to select Unipolar or Bipolar operation for channel 5
J21	Used to select Unipolar or Bipolar operation for channel 4
J22	Used to select Unipolar or Bipolar operation for channel 3
J23	Used to select Unipolar or Bipolar operation for channel 2
J24	Used to select Unipolar or Bipolar operation for channel 1
J25	Used to select Unipolar or Bipolar operation for channel 0
J26	Used to select output voltage span for channel 15
J27	Used to select output voltage span for channel 14
J28	Used to select output voltage span for channel 13
J29	Used to select output voltage span for channel 12

Table continued on the following page

Table 2-1. Jumper Listing (Continued)

Jumper	Function
J30	Used to select output voltage span for channel 11
J31	Used to select output voltage span for channel 10
J32	Used to select output voltage span for channel 9
J33	Used to select output voltage span for channel 8
J34	Used to select output voltage span for channel 7
J35	Used to select output voltage span for channel 6
J36	Used to select output voltage span for channel 5
J37	Used to select output voltage span for channel 4
J38	Used to select output voltage span for channel 3
J39	Used to select output voltage span for channel 2
J40	Used to select output voltage span for channel 1
J41	Used to select output voltage span for channel 0
J42	Select straight/offset binary or two's compliment for channel 15
J43	Select straight/offset binary or two's compliment for channel 13
J44	Select straight/offset binary or two's compliment for channel 11
J45	Select straight/offset binary or two's compliment for channel 9
J46	Select straight/offset binary or two's compliment for channel 7
J47	Select straight/offset binary or two's compliment for channel 5
J48	Select straight/offset binary or two's compliment for channel 3
J49	Select straight/offset binary or two's compliment for channel 1
J50*	Used to select voltage or current mode for channel 15
J51*	Used to select voltage or current mode for channel 14
J52*	Used to select voltage or current mode for channel 13
J53*	Used to select voltage or current mode for channel 12
J54*	Used to select voltage or current mode for channel 11
J55*	Used to select voltage or current mode for channel 10
J56*	Used to select voltage or current mode for channel 9
J57*	Used to select voltage or current mode for channel 8
J58*	Used to select voltage or current mode for channel 7
J59*	Used to select voltage or current mode for channel 6
J60*	Used to select voltage or current mode for channel 5
J61*	Used to select voltage or current mode for channel 4
J62*	Used to select voltage or current mode for channel 3
J63*	Used to select voltage or current mode for channel 2
J64*	Used to select voltage or current mode for channel 1
J65*	Used to select voltage or current mode for channel 0

* Used on the 531/2 only

2.5 VMEbus OPTIONS

The XVME-531 is designed to be addressed within either the VMEbus Short I/O or Standard Memory Space. Since each module connected to the bus must have its own unique base address, the base addressing scheme for XVME I/O modules is designed to be switch selectable. When the XVME-531 is installed into the system, it will occupy a 1 Kbyte block of Short I/O or Standard Address Memory Space.

The Xycom base address decoding scheme for input modules is such that the starting address for the module will always reside on a 1 Kbyte boundary. Thus, the module base address may be set for any one of 64 possible 1 Kbyte boundaries within the Short I/O Address Space or any 1 Kbyte boundary within the upper 64 Kbytes of the VMEbus Standard Address Space (FF0000-FFFC00).

Table 2-2. VMEbus Options

VMEbus OPTIONS	
Switch 1	**Used to configure address**
Position 1-6	Module base address select jumpers. Refer to Section 2.5.1.
Position 7	This switch position determines whether the module will respond to only supervisory access or to both supervisory and non-privileged accesses. Refer to Section 2.5.2.
Position 8	This switch position determines whether the module will reside in the short I/O address space or FFXXXX in the standard address space. Refer to Section 2.5.3

Table 2-3. VMEbus Jumper Options

VMEbus Options	
Jumper	**Use**
J1	Used to enable or disable SYSFAIL*

2.5.1 **Base Address Selection Switch (Switch 1)**

The module base address is selected by using switch 1, positions 1-6. Figure 2-2 shows how each switch position relates to the address lines.

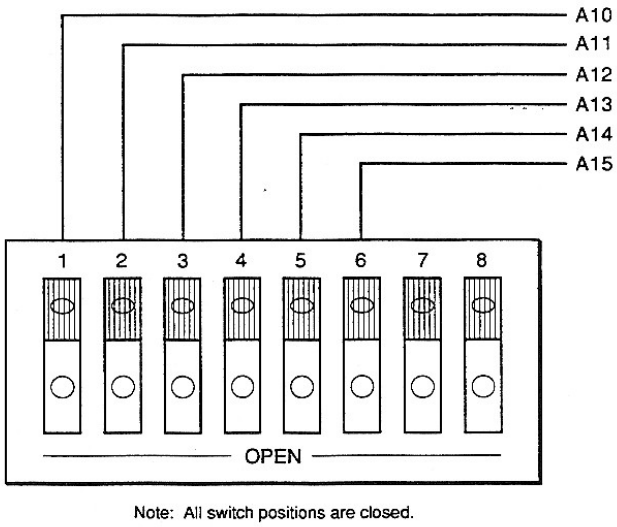


Figure 2-2. Base Address Switch 1

When the switch position is closed, the corresponding base address bit will be logic 0. When the switch position is open, the corresponding base address bit will be logic 1.

Table 2-4 shows a list of the 64 1-Kbyte boundaries which can be used as module base addresses in both the Short I/O and Standard Address Space (as well as the corresponding switch settings for each address).

Table 2-4. Base Address Settings Switch 1

Switch 1 Position						BaseAddress of Module (Hex)
6	5	4	3	2	1	
0	0	0	0	0	0	0000
0	0	0	0	0	1	0400
0	0	0	0	1	0	0800
0	0	0	0	1	1	0C00
0	0	0	1	0	0	1000
0	0	0	1	0	1	1400
0	0	0	1	1	0	1800
0	0	0	1	1	1	1C00
0	0	1	0	0	0	2000
0	0	1	0	0	1	2400
0	0	1	0	1	0	2800
0	0	1	0	1	1	2C00
0	0	1	1	0	0	3000
0	0	1	1	0	1	3400
0	0	1	1	1	0	3800
0	0	1	1	1	1	3C00
0	1	0	0	0	0	4000
0	1	0	0	0	1	4400
0	1	0	0	1	0	4800
0	1	0	0	1	1	4C00
0	1	0	1	0	0	5000
0	1	0	1	0	1	5400
0	1	0	1	1	0	5800
0	1	0	1	1	1	5C00
0	1	1	0	0	0	6000
0	1	1	0	0	1	6400
0	1	1	0	1	0	6800
0	1	1	0	1	1	6C00
0	1	1	1	0	0	7000
0	1	1	1	0	1	7400
0	1	1	1	1	0	7800
0	1	1	1	1	1	7C00
1	0	0	0	0	0	8000
1	0	0	0	0	1	8400
1	0	0	0	1	0	8800
1	0	0	0	1	1	8C00
1	0	0	1	0	0	9000
1	0	0	1	0	1	9400
1	0	0	1	1	0	9800
1	0	0	1	1	1	9C00
1	0	1	0	0	0	A000
1	0	1	0	0	1	A400
1	0	1	0	1	0	A800
1	0	1	0	1	1	AC00

Open = Logic "1"
Closed = Logic "0"

Table 2-4. Base Address Settings Switch 1 (Continued)

Switch 1 Position						**Base Address** of Module
6	5	4	3	2	1	(Hex)
1	0	1	1	0	0	B000
1	0	1	1	0	1	B400
1	0	1	1	1	0	B800
1	0	1	1	1	1	BC00
1	1	0	0	0	0	C000
1	1	0	0	0	1	C400
1	1	0	0	1	0	C800
1	1	0	0	1	1	CC00
1	1	0	1	0	0	D000
1	1	0	1	0	1	D400
1	1	0	1	1	0	D800
1	1	0	1	1	1	DC00
1	1	1	0	0	0	E000
1	1	1	0	0	1	E400
1	1	1	0	1	0	E800
1	1	1	0	1	1	EC00
1	1	1	1	0	0	F000
1	1	1	1	0	1	F400
1	1	1	1	1	0	F800
1	1	1	1	1	1	FC00

Open = Logic "1"
Closed = Logic "0"

2.5.2 **Supervisor/Non-privileged Mode Selection (Switch 1 Position)**

To configure the XVME-531 to respond only to supervisory accesses, open switch 1 position 7. For the module to respond to both supervisory and non-privileged accesses, close switch 1 position 7 (default configuration). Refer to Table 2-5 for more information.

2.5.3 **Short I/O or Standard Address Selection**

To select the VMEbus Short I/O address space, close switch 1 position 8 (default configuration). To select Standard memory space, open switch 1 position 8. If Standard data access is chosen, address bits A23 - A16 will be FFH. Refer to Table 2-5 for more information.

2.5.4 **Address Modifier Reference**

Table 2-5 indicates the VMEbus address modifier code that the XVME-531 will respond to, based on the status of the two options discussed in the previous two sections.

Table 2-5. Address Modifier Code Options

Address Space	**Switch 1**		**Address Modifier Code**	**Access Mode**
	Pos 7	**Pos 8**		
Short I/O	Open	Closed	2DH only	Supervisory Only
	Closed	Closed	29H and 2DH	Supervisory or Non-privileged
Standard	Open	Open	3DH only	Supervisory Only
	Closed	Open	39H and 3DH	Supervisory or Non-privileged

2.5.5 **SYSFAIL Jumper (J1)**

The position of jumper (J1) determines whether the XVME-531 can assert a SYSFAIL*. When J1A is selected, the SYSFAIL* driver is disabled. When J1B is selected, the SYSFAIL* driver is enabled, and the module will assert SYSFAIL* when the Red (fail) LED is on. J1A is the factory shipped configuration. Refer to Section 3.3.2.1 on how to activate SYSFAIL*.

2.6 DIGITAL TO ANALOG CONVERSION OPTIONS

Table 2-6. Digital to Analog Conversion Jumper Options

DIGITAL TO ANALOG CONVERSION OPTIONS	
Jumper	**Use**
J2 - J9, and J42 - J49	These jumpers provide the option to individually configure each output channel to convert either straight binary to analog or to convert two's complement binary to analog.
J10 - J41	These groups of jumpers select one of three output voltage ranges for each output channel. One of these jumpers also activate calibration potentiometers (specific to each channel) to provide for the adjustment of either unipolar offset or for the adjustment of bipolar offset voltage.
J50 - J65	On the XVME-531/2 only, these jumpers configure the 16 output channels to convert data to either an analog voltage format or an analog current format. Refer to Section 2.6.3.

2.6.1 **Output Conversion Format Jumpers (J2 - J9, J42 - J49)**

This jumper option provides a means of configuring the D/A conversion circuitry to handle digital data in either the straight/offset binary formats or in the two's complement binary format. The use of this option is entirely dependent upon the data format which is provided by the output control program being employed by the user. Each of the 16 output channels can be configured independently as shown in Table 2-7.

Table 2-7. Output Conversion Format Jumpers

Output Channel	**Digital Data Conversion Formats**	
	Straight/Offset Binary	**Two's Complement**
0	J9A	J9B
1	J49A	J49B
2	J8A	J8B
3	J48A	J48B
4	J7A	J7B
5	J47A	J47B
6	J6A	J6B
7	J46A	J46B
8	J5A	J5B
9	J45A	J45B
10	J4A	J4B
11	J44A	J44B
12	J3A	J3B
13	J43A	J43B
14	J2A	J2B
15	J42A	J42B

2.6.2 **Output Voltage Range Selection Jumpers (J10-J41)**

All 16 output channels can be jumper-configured to provide analog output voltages in any one of three voltage ranges. There are two bipolar output voltage ranges and one unipolar output voltage range.

The bipolar ranges are:

±5V
±10V

The unipolar range is:

0 to +10V

Each output channel has its own group of two jumpers which determine which of the three output voltage ranges will apply to that channel. In addition, each output channel has a corresponding jumper which activates an offset voltage calibration potentiometer, and thus, allows offset adjustment for either bipolar or unipolar operation. Table 2-8 shows the various jumper combinations used to configure the output channels for the specific voltage ranges.

NOTE
The last jumper in each group (J26 - J41) is the jumper which activates the offset voltage calibration potentiometer for either unipolar or bipolar adjustment on each channel. Refer to Chapter 4 for the calibration procedure.

Table 2-8. Output Voltage Range Configurations

Channel	Jumper	Output Voltage Ranges		
		0 - 10V	**+ / 5V**	**+ / - 10V**
0	J25 J41	B B	A B	A A
1	J24 J40	B B	A B	A A
2	J23 J39	B B	A B	A A
3	J22 J38	B B	A B	A A
4	J21 J37	B B	A B	A A
5	J20 J36	B B	A B	A A
6	J19 J35	B B	A B	A A
7	J18 J34	B B	A B	A A
8	J17 J33	B B	A B	A A
9	J16 J32	B B	A B	A A
10	J15 J31	B B	A B	A A
11	J14 J30	B B	A B	A A
12	J13 J29	B B	A B	A A
13	J12 J28	B B	A B	A A
14	J11 J27	B B	A B	A A
15	J10 J26	B B	A B	A A

NOTE

On the XVME-531/2, when using a channel in the current output mode, the voltage output range jumpers for that channel must be configured for the 0-10V range. (Refer to Section 2.6.3).

Before the XVME-531 Analog Output Module is shipped from the factory, it is configured and calibrated for the following output ranges:

XVME-531/1	-	Straight Binary Unipolar 0-10V Voltage Output
XVME-531/2	-	Straight Binary Unipolar 4-20mA Current Output

2.6.3 **Voltage/Current Output Selection Jumpers (J50 - J65) (531/2 Only)**

In case of the XVME-531/2, each of the 16 analog output channels is capable of providing an output which can be used as either a voltage applied source or a current applied source (refer to Section 1.1 of Chapter 1 for information on the difference between the XVME-531/1 and the XVME-531/2). Prior to configuring any other channel specific criteria, it should be determined whether the D/A channel will be used as an analog voltage source or as an analog current source. Table 2-9 shows which jumpers configure the channels as current outputs, and which jumpers configure the channels as voltage outputs.

Table 2-9. Voltage/Current Output Selection Jumpers
(XVME-531/2 Option Only)

Output Channel	**Output**	
	Voltage	**Current**
0	J65A	J65B
1	J64A	J64B
2	J63A	J63B
3	J62A	J62B
4	J61A	J61B
5	J60A	J60B
6	J59A	J59B
7	J58A	J58B
8	J57A	J57B
9	J56A	J56B
10	J55A	J55B
11	J54A	J54B
12	J53A	J53B
13	J52A	J52B
14	J51A	J51B
15	J50A	J50B

When a channel is to be configured for voltage output, a corresponding voltage range must be selected and jumpered (refer to Section 2.6.2). Depending on whether the voltage range selected is unipolar or bipolar, a channel specific potentiometer is jumper selected (refer to Section 2.6.2) and voltage offset calibration can be performed (refer to Chapter 4 for calibration information).

When the channel is configured for current output on the XVME-531/2, the voltage range selection jumpers which correspond to that particular channel **must** be configured for the 0-10V range (see the note in Section 2.6.2). The specified current loop range for each output channel is 4-20mA.

2.7 EXTERNAL CONNECTORS P3 AND P4

The analog output channels are accessible on the front panel of the module in the form of two single mass termination headers (labeled P3 and P4). Connector P4 contains channels 0-7 while P3 contains channels 8-15.

Figure 2-3 shows the module (XVME-531) front panel and how the pins are situated in the connector.

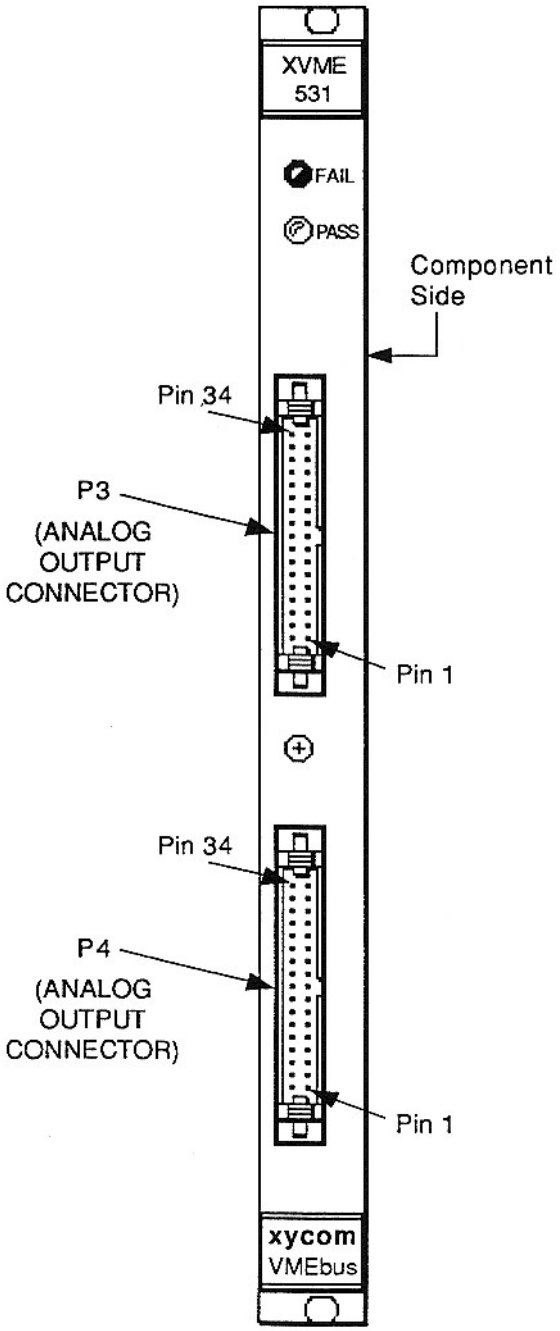


Figure 2-3. Front Panel Layout

Table 2-10 shows the pin designations for connectors P3 and P4.

Table 2-10. Output Connectors P3 and P4

P4 Connector		P3 Connector	
Pin	**Definition**	**Pin**	**Definition**
1, 5, 9, 13, 17, 21, 25, 29, 33, 34	AGND	1, 5, 9, 13, 17, 21, 25, 29, 33, 34	AGND
2	VOUT CHAN 0	2	VOUT CHAN 8
3	-IOUT CHAN 0	3	-IOUT CHAN 8
4	+IOUT CHAN 0	4	+IOUT CHAN 8
6	VOUT CHAN 1	6	VOUT CHAN 9
7	-IOUT CHAN 1	7	-IOUT CHAN 9
8	+IOUT CHAN 1	8	+IOUT CHAN 9
10	VOUT CHAN 2	10	VOUT CHAN 10
11	-IOUT CHAN 2	11	-IOUT CHAN 10
12	+IOUT CHAN 2	12	+IOUT CHAN 10
14	VOUT CHAN 3	14	VOUT CHAN 11
15	-IOUT CHAN 3	15	-IOUT CHAN 11
16	+IOUT CHAN 3	16	+IOUT CHAN 11
18	VOUT CHAN 4	18	VOUT CHAN 12
19	-IOUT CHAN 4	19	-IOUT CHAN 12
20	+IOUT CHAN 4	20	+IOUT CHAN 12
22	VOUT CHAN 5	22	VOUT CHAN 13
23	-IOUT CHAN 5	23	-IOUT CHAN 13
24	+IOUT CHAN 5	24	+IOUT CHAN 13
26	VOUT CHAN 6	26	VOUT CHAN 14
27	-IOUT CHAN 6	27	-IOUT CHAN 14
28	+IOUT CHAN 6	28	+IOUT CHAN 14
30	VOUT CHAN 7	30	VOUT CHAN 15
31	-IOUT CHAN 7	31	-IOUT CHAN 15
32	+IOUT CHAN 7	32	+IOUT CHAN 15

2.8 INSTALLING THE XVME-531 INTO A CARDCAGE

CAUTION

Do not attempt to install or remove any boards without first turning off the power to the bus, and all related external power supplies.

Prior to installing a module, you should determine and verify all relevant jumper configurations. Check the jumper configuration with the diagram and lists in the manual.

To install a board in the cardcage, do the following:

1. Make certain that the particular cardcage slot which you are going to use is clear and accessible.

2. Center the board on the plastic guides in the slot so that the handle on the front panel is towards the bottom of the cardcage. (Refer to Figure 2-4).

3. Push the card slowly toward the rear of the chassis until the connectors are fully engaged and properly seated.

NOTE

It should not be necessary to use excess force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

4. Once the board is properly seated, tighten the two machine screws at the top and bottom of the front panel.

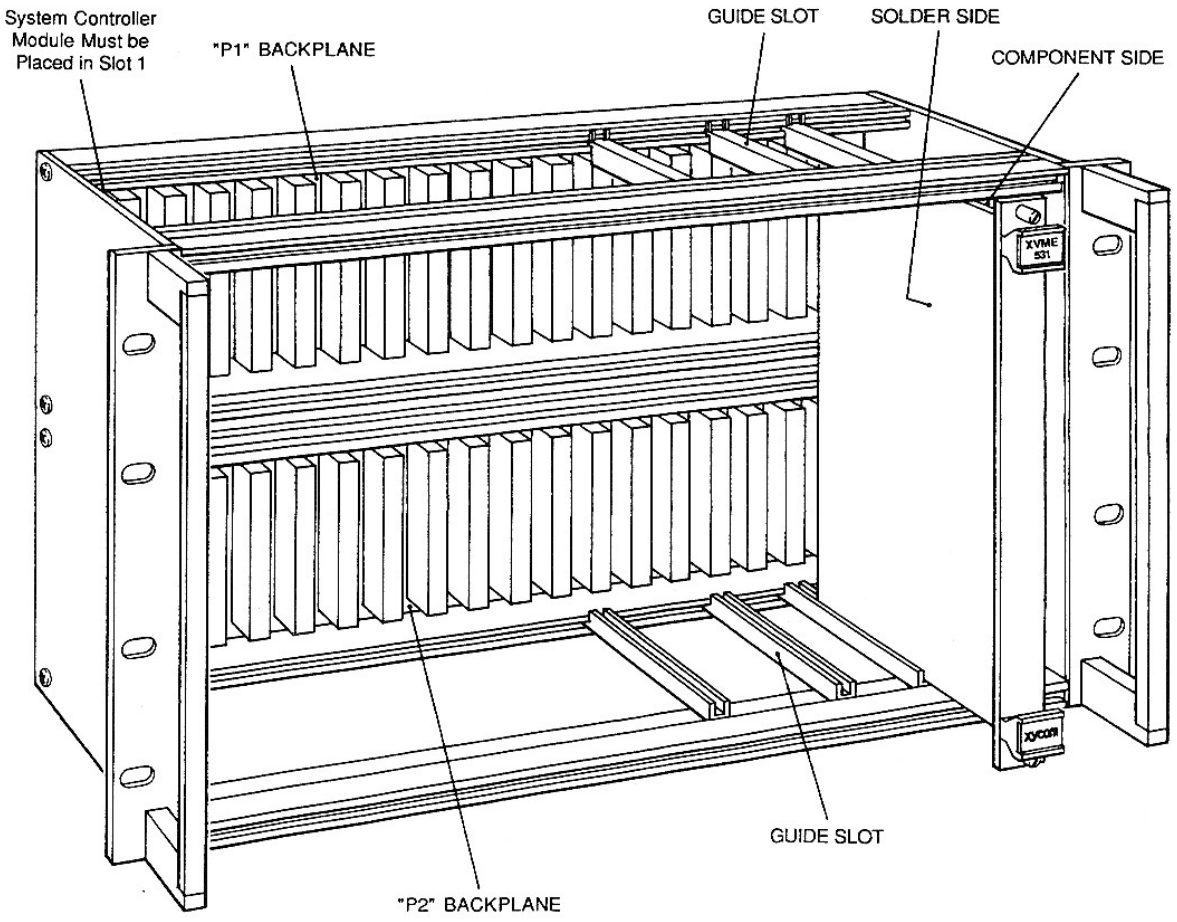


Figure 2-4. VMEbus Chassis

3.1 INTRODUCTION

This chapter provides information required to program the XVME-531 Analog Output Module for analog output operations. The information is presented in the following order:

- Base addressing
- Module address map with programming locations and descriptions of registers
- Resetting of data format module

3.2 MODULE BASE ADDRESSING

The XVME-531 Analog Output Module is designed to be addressed within either the VMEbus-defined 64 Kbyte Short I/O Address Space or the upper 64 Kbytes of the Standard Address Space (FF0000H - FFFC00H). Because each I/O module connected to the bus must have a unique base address, the addressing scheme for Xycom XMVE-I/O modules is configurable. When the XVME-531 is installed in a system, it will occupy a 1 Kbyte block of address space (also referred to as I/O block)

The base address decoding scheme for the XVME-531 positions the starting address of each board on a 1 Kbyte boundary. Thus, there are 64 possible base addresses (1 Kbyte boundaries) for the XVME-531 within either the Short I/O Address Space or the upper 64 Kbytes of Standard Address Space. (Refer to Table 2-4 for a list of base addresses and their corresponding SW1 bit locations.)

Figure 3-1 shows a memory map for the XVME-531 (all address numbers are hexadecimal).

	Even	Odd	
Base +00H 3EH			01H 3FH
	Undefined	Identification	
40H 7EH	Reserved	Reserved	41H 7FH
80H	Undefined	Status/Control	81H
82H 86H	Undefined	Undefined	83H 87H
88H	Channel 0 D/A High	Channel 0 D/A Low	89H
8AH	Channel 1 D/A High	Channel 1 D/A Low	8BH
8CH	Channel 2 D/A High	Channel 2 D/A Low	8DH
8EH	Channel 3 D/A High	Channel 3 D/A Low	8FH
90H	Channel 4 D/A High	Channel 4 D/A Low	91H
92H	Channel 5 D/A High	Channel 5 D/A Low	93H
94H	Channel 6 D/A High	Channel 6 D/A Low	95H
96H	Channel 7 D/A High	Channel 7 D/A Low	97H
98H	Channel 8 D/A High	Channel 8 D/A Low	99H
9AH	Channel 9 D/A High	Channel 9 D/A Low	9BH
9CH	Channel 10 D/A High	Channel 10 D/A Low	9DH
9EH	Channel 11 D/A High	Channel 11 D/A Low	9FH
A0H	Channel 12 D/A High	Channel 12 D/A Low	A1H
A2H	Channel 13 D/A High	Channel 13 D/A Low	A3H
A4H	Channel 14 D/A High	Channel 14 D/A Low	A5H
A6H	Channel 15 D/A High	Channel 15 D/A Low	A7H
A8H C6H	Reserved		A9H C7H
C8H E6H			C9H E7H
E8H	Channel 0-15 Update Register		E9H
EAH FEH			EBH FFH
	Reserved		

Figure 3-1. XVME-531 Memory Map

A specific register on the module can be accessed by adding the specific register offset to the module base address. For example, the module status/control register is located at address 81H within the I/O interface block. However, if the module base address is jumpered to 1000H, the status/control register would be accessible at address 1081.

(Module base address)	**(Register offset)**	**(Status/Control Register)**
1000H	**+ 81H**	**= 1081H**

For memory-mapped CPU modules, the short I/O address space is memory-mapped to begin at a specific address. For such modules, the module base address is an offset from the start of this memory-mapped short I/O address space. For example, assume the short I/O address space of a CPU module starts at F90000H, and if the base address of the XVME-531 is set a 1000H, the actual module base would be F91000H.

3.3 MODULE ADDRESS MAP AND DESCRIPTION OF REGISTERS

Each of the following programming locations of the XVME-531 is defined in this section.

Module Identifier (base + 01H/3FH)
This includes information concerning the locations specifying model number, manufacturer, and revision levels of the module.

Status/Control Register (base + 81H)
The status/control register provides the control signals required to reset the module, select the mode of operation, monitor the busy bit, and control the pass and fail LEDs. Table 3-2 shows the bits in the status/control register.

Multi-channel Update Register (base + E8H/E9H)
This register is used to update multiple D/A channels simultaneoulsy.

D/A Channel Registers *(base + 88H - A7H)*
These registers have individual address locations for each D/A channel (12 bit register).

NOTE
Reading from or writing to undefined I/O interface block locations may make application software incompatible with future XVME modules.

3.3.1 **Module Identification Information (Base + 01H)**

The Xycom module identification information for the XVME-531 is located in the odd bytes at addresses 01H to 3FH. The I.D. data is provided as 32 ASCII encoded characters consisting of board type, manufacturer identification, module model number, number of 1 Kbyte blocks occupied by the module, and module revision level. This information can be read by the system processor on power-up to verify the system configuration and operational status. Table 3-1 defines the identification information locations.

Table 3-1. Module I.D. Data

Offset Relative to Module Base	Contents	ASCII Encoding in Hex	Descriptions
1	V	56	ID PROM identifier,
3	M	4D	always "VMEID"
5	E	45	(5 characters)
7	I	49	
9	D	44	
B	X	58	Manufacturer's I.D.
D	Y	59	
F	C	43	Modules (3 characters)
11	5	35	
13	3	33	Module model number
15	1	31	(4 characters and
17	*1, 2	31, 32	3 trailing blanks)
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1 Kbyte blocks of I/O space occupied by this module (1 character)
21		20	Major functional revision level
23	1	31	with leading blank (if single digit)
25	1	30	Minor functional revision
27		20	level with trailing blank (if single digit)
29	Undefined	00	
2B	Undefined	00	
2D	Undefined	00	
2F	Undefined	00	
31	Undefined	00	
33	Undefined	00	
35	Undefined	00	Manufacturer-dependent
37	Undefined	00	information, reserved for
39	Undefined	00	future use
3B	Undefined	00	
3D	Undefined	00	
3F	Undefined	00	

* 1 if 531/1, 2 if 531/2

Each module I.D. data location is accessed only by odd VME addresses. The 32 bytes of ASCII data are assigned to the first 32 odd I/O interface block bytes. This allows I.D. information to be accessed by addressing the module base, offset by the specific address for the characters needed.

3.3.2 **Status/Control Register (Base + 81H)**

The status/control register provides the control signals required to reset the module, select the mode of operation, monitor the busy bit, and control the pass and fail LEDs. Table 3-2 shows the bits in the status/control register.

Table 3-2. Status/Control Register (Base + 81H)

BIT #	**FUNCTION**	
	STATUS	**CONTROL**
D0	SYSFAIL (Red LED)	SYSFAIL (Red LED)
D1	PASS (Green LED)	PASS (Green LED)
D2	Not Used	Not Used
D3	Not Used	Not Used
D4	Module Reset	Module Reset
D5	Mode Bit	Mode Bit
D6	Not Used	Not Used
D7	D/A Busy	Not Used

3.3.2.1 **Status/Control Register Bit Definitions**

D7 **Used on 531/2 only.** This busy bit should be monitored to find out exactly when the data has passed through the Opto isolators and has been latched by the D/A channel. A logic "1" in the busy bit indicates that the XVME-531 is in the process of writing to one of the D/A channels. Logic 1 is present until the data and control signals have passed through the Opto isolators and the channel has been latched (approximately 12 us). This bit is used only on isolated versions of the XVME-531 and only when data is going across the Opto isolators (any write or update to a D/A channel will pass through the Opto isolators. The control register may be written to while the busy bit is high, however, the mode bit shouldn't be changed during this time.

Also, any register location on board may be read during this time including the D/A channel register since the data is read from a RAM on board and not the D/A channel itself. For the non-isolated version (tab 001), data is written to the D/A channels during the VME cycle so there is no need to monitor this busy bit.

NOTE

Any time a channel is written to, the busy bit should be monitored regardless of whether the D/A channel is actually being updated or whether a D/A channel register is just being written to. If another write to a D/A channel register is started while the busy bit is still high, then the XVME-531 will hold off DTACK until the D/A write cycle that was running is completed. After the previous cycle has completed, then the new cycle will start and the board will DTACK. In this way, you are insured that the cycle that was running will complete before the new cycle starts.

D6 Not used

D5 This Mode Bit is used to initialize the board for one of two modes (0 - transparent mode, 1 - multi-channel mode). See Section 3.4 for a detailed description of these modes.

D4 This Reset Bit is a software module reset. Setting this Bit to "1" resets each analog channel to 000H (800H if two's complement is selected). This bit must be held high for a minimum of 4 uS.

NOTE
Setting this bit does not reset the status/control register. Also, this bit must be reset back to "0" to release the XVME-531 from the reset state.

A software reset brings the output of D/As, from their value at the time, to 000H after reset (what the actual voltage 000H corresponds to depends on how the channel is configured, (see note below).

VME SYSRESET and power-up reset works in the same way with the same delay but the status/control register also gets reset to '0'. During a power-up reset, the voltage on the output of the D/As are not guaranteed until
after DC/DC's U9 and U10 power-up to ±15V.

NOTE
If the channel is configured for the unipolar mode, a reset will cause the analog output to go to 0V. If the channel is jumpered for bipolar mode and two's compliment, then the analog output will also go to 0V. If the channel is jumpered for bipolar mode and offset binary, then the analog output will go to minus full scale.

D3 Not used

D2 Not used

D1, D0 These bits control the red and green LEDs. The red and green LEDs provide visual indication of the XVME-531 status.

A logic "0" turns on the red LED (D0)
A logic "1" turns on the green LED (D1)

The following table shows the LEDs and where they should be used as set forth by the Xycom architecture.

Table 3-3. Pass/Fail LEDs

Status **D1**	**Bits** **D0**	**LEDs** **Green**	**Red**	**SYSFAIL***	**Status**
0	0	Off	On	Active**	Module failed or not yet tested
0	1	Off	Off	Inactive	Inactive module
1	0	On	On	Active**	Module under test
1	1	On	Off	Inactive	Module passed test

** SYSFAIL* will be active if the SYSFAIL* enable/disable jumper is set to the enabled position. Otherwise, it will be inactive. (Refer to Section 2.5.5.)

3.3.3 **D/A Conversion Registers**

The D/A converters can produce a voltage output (and/or a current output on the XVME-531/2) for any of the 16 available output channels. The value of the analog output will be a fraction of the converters "full scale" output, defined by the digital code sent to the converter.

Each output channel (16 total) has its own unique word address starting at location 88H and 89H for channel 0 and ending at location A6H and A7H for channel 15 (see the Memory Map, Figure 3-1). Each channel can be written as a byte or word. The **even** byte contains data bits 8-11 while the **odd** bytes contain data bits 0-7.

Double Buffering
The D/A converters used are double buffered. Double buffering allows the D/A registers to be written without affecting the output of the D/A channel. This feature is used to create two different modes of operation as described in Section 3.4.

3.3.4 **Channel 0-15 Update Register (Location Base +E8, E9)**

The channel update register is used along with the mode bit in the status/control register to update multiple D/A channels simultaneously.

When Mode Bit = 0
When the mode bit is "0", transparent mode is selected and this register serves no purpose.

When Mode Bit = 1
When the mode bit is "1", the multi-channel update mode is selected and this register is used to update the outputs of one or more D/A channels simultaneously. This register can also be read. See Section 3.4 for an explanation of how to use this register.

The table below shows this register along with its bit definition.

Table 3-4. Update Register/Bit Definition

Address	BIT	CHANNEL	DEFINITION
E9	0	Channel 0 Update Bit	1 = Update Chan 0 = No Update
E9	1	Channel 1 Update Bit	1 = Update Chan 0 = No Update
E9	2	Channel 2 Update Bit	1 = Update Chan 0 = No Update
E9	3	Channel 3 Update Bit	1 = Update Chan 0 = No Update
E9	4	Channel 4 Update Bit	1 = Update Chan 0 = No Update
E9	5	Channel 5 Update Bit	1 = Update Chan 0 = No Update
E9	6	Channel 6 Update Bit	1 = Update Chan 0 = No Update
E9	7	Channel 7 Update Bit	1 = Update Chan 0 = No Update
E8	0	Channel 8 Update Bit	1 = Update Chan 0 = No Update
E8	1	Channel 9 Update Bit	1 = Update Chan 0 = No Update
E8	2	Channel 10 Update Bit	1 = Update Chan 0 = No Update
E8	3	Channel 11 Update Bit	1 = Update Chan 0 = No Update
E8	4	Channel 12 Update Bit	1 = Update Chan 0 = No Update
E8	5	Channel 13 Update Bit	1 = Update Chan 0 = No Update
E8	6	Channel 14 Update Bit	1 = Update Chan 0 = No Update
E8	7	Channel 15 Update Bit	1 = Update Chan 0 = No Update

NOTE: The update register +E8, and +E9 may be written as a byte or word at a time.

3.4 WRITING/READING AND UPDATING D/A CHANNELS AND MODES OF OPERATION

The two modes of operation available on the XVME-531 are the **transparent** and **multi-channel update** modes. The desired mode is selected by writing to the mode bit in the status/control register (see Section 3.3.2).

3.4.1 Transparent Mode

In the **transparent mode**, each D/A channel is updated individually when the lower (odd) byte of the desired channel is written to. Byte or word transfers are allowed. If all 12 bits are written at once, then that D/A channel register along with the output of the D/A gets updated at once. The following is an example of the transparent mode.

Example:

Configuration	-	531 Module is programmed for transparent mode when: base + 81, bit 5 = 0
	-	Channel 1 is configured for 0-10V operation with straight binary encoding
Action	-	Write word of 800H to channel 1 (base + 8AH)
Result	-	Output of channel 1 goes to half scale or +5V after the write to channel 1

3.4.2 **Multi-channel Update Mode**

In the **multi-channel update mode**, the individual D/A registers are written to both high and low (even and odd) bytes with no update to the D/A channel. Updating the channel or channels is accomplished by writing to location +E8H, +E9H or both with the desired channel's update bit set to 1. See Section 3.3.4 for register bit descriptions).

The act of writing to this register starts the conversion process. One, two or all 16 D/A channels may be updated at once, while in this mode. Also, any combination of these 16 channels may be updated at once. The following shows examples of the multi-channel update mode.

1. Example: Board is in multi-channel mode when: base + 81H, bit 5 = 1

   Channel 0

Configuration:	Unipolar 0-10V, straight binary
Action:	Write word of 400H to channel 0 (+88H, 89H)
Result:	Output of channel 0 will remain where it was
Action:	Write byte 01H to update register +E9H or word of 01H to +E8H
Result:	Output of channel 0 will go to 2.5V after conversion

2. Example:

   Channel 9

Configuration:	± 10 Bipolar two's compliment encoding
Action:	Write word of 100H to channel 9 (+9AH)
Result:	Output of channel 5 is unchanged
Action:	Write word of 0200H to update register (+E8)
Result:	Output of channel 9 will go to 1.25 volts after conversion

3. Example: If all DACs need to be updated at once:

Action:	Load D/A converter registers with desired data for conversion, then write word of FFFFH to update register +E8H.

3.4.3 **Reading D/A Channel Registers**

When a D/A channel register is written to, both RAM and the actual D/A converter register gets written. During a read, **only** the RAM is read.

Since the D/A RAMs power-up with unknown data, the RAM D/As (used for reading D/A registers) must be initialized before they can be read correctly. This is also true for any reset condition (SYSRESET* or a software reset) since the RAM data will remain the same after the reset whereas the actual D/A registers were reset.

> **NOTE**
> When reading a D/A channel, the information read contains the data in the D/A register and not necessarily what the actual output of the D/A channel contains.

3.5 **DIGITAL OUTPUT DATA FORMAT**

The digital data written to the D/A conversion registers corresponds to the magnitude of the analog output signal in a relation that is different for each of the two digital data formats (i.e., Straight/Binary Encoding or Offset Binary Encoding).

The analog output signals can be divided into two general groups:

Unipolar Output - where the output has only a positive polarity (e.g., 0-10V or 4-20mA).

and

Bipolar Output - where the output magnitude can have a negative or positive polarity (e.g., ±5V, ±10V).

> **NOTE**
> When an output is used in current mode (on the XVME-531/2 version only) it is required to be configured as a unipolar 0 - 10V output.

Unipolar Mode

In the unipolar mode, the data to be converted is usually encoded in the Straight Binary format. The following table shows the data encoding for the Straight Binary format in the Unipolar mode.

Table 3-5. Unipolar Mode

X = Don't Care Straight Binary Format Voltage Mode: D_{15} D_0	Analog Output
X X X X 1 1 1 1 1 1 1 1 1 1 1 1 X X X X 1 0 0 0 0 0 0 0 0 0 0 0 X X X X 0 0 0 0 0 0 0 0 0 0 0 0	Vfsr - 1 LSB Vfsr/2 0V
Current Mode (XVME-531/1/2 only): D_{15} D_0	Analog Output 4 - 20mA
X X X X 1 1 1 1 1 1 1 1 1 1 1 1 X X X X 1 0 0 0 0 0 0 0 0 0 0 0 X X X X 0 0 0 0 0 0 0 0 0 0 0 0	19.996mA (20mA - 1 LSB) 12mA 4mA

Bipolar Mode

In the Bipolar Mode, the digital value converted to analog is encoded in either Offset Binary or Two's Complement format.

Offset Binary

In the Offset Binary format, the negative full scale voltage (-Vmax) is represented by all binary zeros. The positive full scale voltage minus one LSB is represented by all binary ones. Thus, the voltage represented is "offset" by a factor of one half of the full scale voltage "swing" (+Vmax to -Vmax).

Two's Complement Format

In Two's Complement format, the most significant bit is simply inverted. This provides for direct mapping between the Two's Complement numbers used by the microprocessor and the voltage output of the digital to analog convertor. Table 3-6 shows the offset and two's complement encoding formats.

Table 3-6. Bipolar Modes

X = Don't Care Offset Binary Format: D_{15} D_0	Analog Output
X X X X 1 1 1 1 1 1 1 1 1 1 1 1 X X X X 1 1 0 0 0 0 0 0 0 0 0 0 X X X X 1 0 0 0 0 0 0 0 0 0 0 0 X X X X 0 1 0 0 0 0 0 0 0 0 0 0 X X X X 0 0 0 0 0 0 0 0 0 0 0 0	+Vfsr - 1 LSB Vfsr/2 0V -Vfsr/2 -Vfsr
Two's Compliment Format: D_{15} D_0	Analog Output
X X X X 1 1 1 1 1 1 1 1 1 1 1 1 X X X X 0 1 0 0 0 0 0 0 0 0 0 0 X X X X 0 0 0 0 0 0 0 0 0 0 0 0 X X X X 1 1 0 0 0 0 0 0 0 0 0 0 X X X X 1 0 0 0 0 0 0 0 0 0 0 0	+Vfsr - 1 LSB 1/2 (+Vfsr) 0V 1/2 (-Vfsr) -Vfsr

Least Significant Bit

The LSB (Least Significant Bit) represents the change in output voltage that is the result of an increase or decrease of the binary code by one count. The LSB is derived from the full range (fsr) of either current or voltage divided by the maximum conversion resolution (i.e., 12 bits or 4096 in binary equivalent). The value of one LSB can be determined by the following:

$$\text{Unipolar LSB} = \frac{\text{Vfsr}}{4096} \qquad \text{Bipolar LSB} = \frac{(+\text{Vfsr}) - (-\text{Vfsr})}{4096}$$

$$\text{Current LSB} = \frac{20\text{mA} - 4\text{mA}}{4096}$$

The following list shows the value of one LSB for each range:

±5V	=	2.4414mV
±10V	=	4.8828mV
0 - 10V	=	2.4414mV
4 - 20mA	=	3.906uA

3.6 D/A CONVERSION PRINCIPLES

A general procedure for configuring the XVME-531 Analog Output Module to convert digital data to analog outputs must include the following elements:

1. Configure jumpers (refer to Chapter 2) for the output voltage range (unipolar or bipolar), digital data conversion format (straight binary or offset binary), D/A converter reset state at power-up or system reset (i.e., the converters are loaded with either all logic "0's" or all logic "1's" at power-up or reset), and in the case of the XVME-531-2, the output type (i.e., voltage or current).

2. Perform Calibration (see Chapter 4).

3. Write data to be converted to the desired 16 bit D/A output register in the byte or word mode. If the data is transferred to the register in the byte mode, the high order byte must be written prior to the low order byte.

   Transparent Mode
   When the low order byte is written, the D/A conversion is initiated and the output will change state.

   Multi-channel Mode
   When the update register is written with the desired update bits set, the D/A conversion will be initiated for those channels.

3.7 CURRENT LOOP OUTPUTS ON THE XVME-531/2

When the outputs on the XVME-531/2 are configured for current loop operation, the loop supply voltage is provided by an on-board ±15V DC-DC converter circuit. This converter not only generates ±15V from the VMEbus supplied +5V, but it also serves to separate analog ground from the digital ground. The D/A outputs are capable of handling current loop configurations in the 4-20mA range with a loop resistance range of 50-525 ohms. Analog ground is used for the current return.

When used in the current output mode, the output channels on the XVME-531/2 **must** be configured for the 0-10V output range.

3.8 RESETTING OF MODULE

There are three ways to reset the module:

- Power-up reset
- VME SYSRESET*
- Software Reset (see Section 3.3.2)

3.8.1 Affects of Resetting

The D/A output for the following configuration is affected when powering-up, SYSRESET* or Software Reset:

Table 3-7. D/A Output Affected

Jumpered For	Digital Reset Value	Analog Reset Value
Unipolar 0-10V straight binary	000H	0V
Unipolar 4-20mA straight binary 531/2	000H	4mA
Bipolar ±5V offset binary	000H	-5V
Bipolar ±5V two's compliment	800H	0V
Bipolar ±10V offset binary	000H	-10V
Bipolar ±10V two's compliment	800H	0V

NOTE
The outputs of the D/A channels are not guaranteed to be valid until 50mS after the +5V has been powered-up.

3.8.2 **Resetting Status/Control Register**

The status/control register powers-up as 00H. SYSRESET will also reset this register to 00H, however, Software Reset has no affect on this register.

3.8.3 **Resetting Update Register**

Any Reset (Power-up, SYSRESET and Software Reset) will reset the update register to 0000H.

3.9 **ISOLATION ON THE XVME-531/2**

The XVME-531/2 board is rated for 500 Volts of isolation between the analog section, and the VMEbus. Opto-isolators are used to pass the control signals and the databus to the analog section. Because of this, a busy bit is needed to be monitored when the data has been transferred to the analog section. See Section 3.3.2 for more information.

4.1 INTRODUCTION

Calibration facilities have been provided on the XVME-531 for each D/A channel. It is recommended that any time the module is reconfigured (i.e., configuration jumpers are changed), that the calibration be checked and adjusted if necessary.

The calibration procedure entails offset and gain adjustment for the output channels in either the unipolar or the bipolar modes of operation.

Locations of the calibration potentiometers can be found in Figure 4-1.

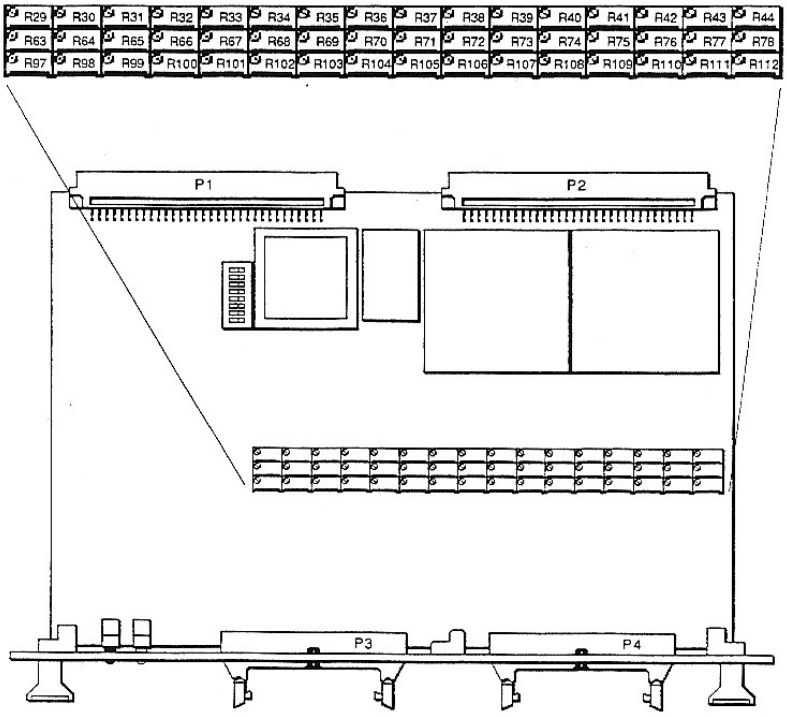


Figure 4-1. Potentiometer Locations

4.2 D/A CALIBRATION PROCEDURE

The output calibration procedure is detailed in Table 4-1, showing the potentiometers used for output calibration.

Table 4-1. D/A Calibration Potentiometers

Resistor	Description
R112 R78 R44	Channel 0 Unipolar Adjustment Channel 0 Bipolar Adjustment Channel 0 Gain Adjustment
R111 R77 R43	Channel 1 Unipolar Adjustment Channel 1 Bipolar Adjustment Channel 1 Gain Adjustment
R110 R76 R42	Channel 2 Unipolar Adjustment Channel 2 Bipolar Adjustment Channel 2 Gain Adjustment
R109 R75 R41	Channel 3 Unipolar Adjustment Channel 3 Bipolar Adjustment Channel 3 Gain Adjustment
R108 R74 R40	Channel 4 Unipolar Adjustment Channel 4 Bipolar Adjustment Channel 4 Gain Adjustment
R107 R73 R39	Channel 5 Unipolar Adjustment Channel 5 Bipolar Adjustment Channel 5 Gain Adjustment
R106 R72 R38	Channel 6 Unipolar Adjustment Channel 6 Bipolar Adjustment Channel 6 Gain Adjustment
R105 R71 R37	Channel 7 Unipolar Adjustment Channel 7 Bipolar Adjustment Channel 7 Gain Adjustment
R104 R70 R36	Channel 8 Unipolar Adjustment Channel 8 Bipolar Adjustment Channel 8 Gain Adjustment
R103 R69 R35	Channel 9 Unipolar Adjustment Channel 9 Bipolar Adjustment Channel 9 Gain Adjustment
R102 R68 R34	Channel 10 Unipolar Adjustment Channel 10 Bipolar Adjustment Channel 10 Gain Adjustment
R101 R67 R33	Channel 11 Unipolar Adjustment Channel 11 Bipolar Adjustment Channel 11 Gain Adjustment

Table 4-1. D/A Calibration Potentiometers (Continued)

Resistor	Description
R100 R66 R32	Channel 12 Unipolar Adjustment Channel 12 Bipolar Adjustment Channel 12 Gain Adjustment
R99 R65 R31	Channel 13 Unipolar Adjustment Channel 13 Bipolar Adjustment Channel 13 Gain Adjustment
R98 R64 R30	Channel 14 Unipolar Adjustment Channel 14 Bipolar Adjustment Channel 14 Gain Adjustment
R97 R63 R29	Channel 15 Unipolar Adjustment Channel 15 Bipolar Adjustment Channel 15 Gain Adjustment

The following equipment is required to perform output calibration:

- A 5-digit volt meter capable of reading ±30 uV
- A small flat-bladed screw driver

Output calibration entails voltage **offset adjustment** and **gain adjustment** for each channel, in both the unipolar and bipolar configurations.

1. **Offset Adjustment**
   First, offset adjust the D/A channel for the -FS reading by writing out to the D/A channel with the proper digital output to get the -FS reading (refer to Table 4-2).

2. Next, adjust the unipolar or bipolar offset POT (depending on how the channel is configured). Refer to Table 4-1 for POT selection.

Table 4-2. D/A -FS Calibration Points

-FS CALIBRATION			
Binary Encoding Mode	**Voltage Range**	**Digital Data In**	**Analog Value Out (-FS)**
UNIPOLAR (Straight Binary	4-20mA 0-10V	000H 000H	4mA 0V
BIPOLAR (Offset Binary)	±5V ±10V	000H 000H	-5V -10V
BIPOLAR (Two's Complement)	±5V ±10V	0800H 0800H	-5V -10V

3. **Gain Adjustment**
   Then write out to the D/A channel with the proper digital output to get the +FS - 1 LSB reading (refer to Table 4-3).

4. **Potentiometer (POT)**
   Finally, adjust the proper gain POT to the +FS voltage - 1 LSB. Refer to Table 4-1 for POT selection.

Table 4-3. D/A +FS Calibration Points

+FS CALIBRATION			
Binary Encoding Mode	**Voltage Range**	**Digital Data In**	**Analog Voltage Out (+FS - LSB)**
UNIPOLAR (Straight Binary	4-20mA 0-10V	0FFFH 0FFFH	19.9961mA 9.9976V
BIPOLAR (Offset Binary)	±5V ±10V	0FFFH 0FFFH	4.9976V 9.9951V
BIPOLAR (Two's Complement)	±5V ±10V	07FFH 07FFH	4.9976V 9.9951V

Appendix A - **XYCOM STANDARD I/O ARCHITECTURE**

A.1 INTRODUCTION

This Appendix defines XYCOM's Standard I/O Architecture for XVME I/O modules. This Standard I/O Architecture has been incorporated on all XVME-I/O modules in order to provide a simple and consistent method of programming the entire module line. The I/O Architecture specifies the logical aspects of bus interfaces, as opposed to the "physical" or electrical aspects as defined in the VMEbus specifications. The module elements which are standardized by the Xycom I/O Architecture are listed below:

- **Module Addressing -** Where a module is positioned in the I/O address space and how software can read from or write to it.
- **Module Identification -** How software can identify which modules are installed in a system.
- **Module Operational Status -** How the operator can (through software) determine the operational condition of specific modules within the system.
- **Communication Between Modules -** How master (host) processors and intelligent I/O modules communicate through shared global memory or the dual-access RAM on the I/O modules.

A.2 MODULE ADDRESSING

All Xycom I/O modules are designed to be addressed within the VMEbus-defined 64 Kbyte short I/O address space. The restriction of I/O modules to the short I/O address space provides separation of program/data address space and the I/O address space. This convention simplifies software design and minimizes hardware and module cost, while at the same time, providing 64 Kbytes of address space for I/O modules.

A.2.1 **Base Addressing**

Since each I/O module connected to the bus must have its own unique base address, the base addressing scheme for Xycom VME I/O modules has been designed to be switch-selectable. Each XVME-I/O module installed in the system requires at least a 1 Kbyte block of the short address space. Thus, each I/O module has a base address that starts on a 1 Kbyte boundary. As a result, the Xycom I/O modules have all been implemented to decode base addresses in 1 Kbyte (400H) increments.

Figure A-1 shows an abbreviated view of the short I/O memory.

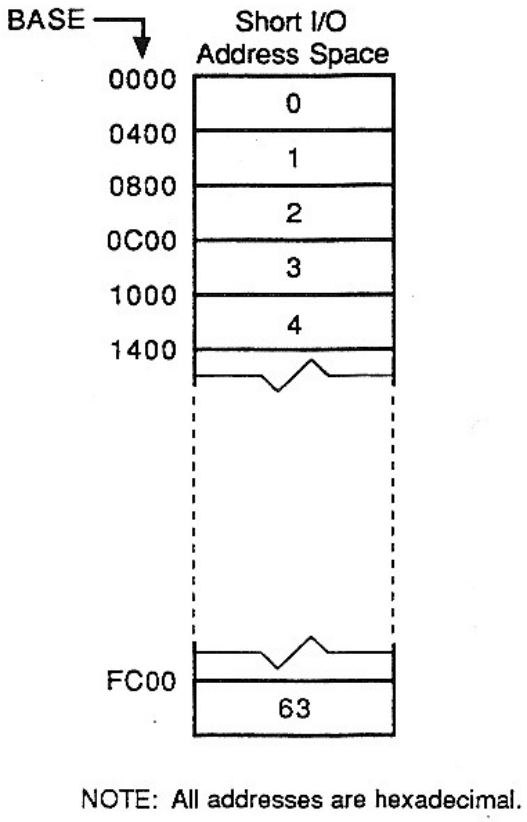


Figure A-1. 64 Kbyte Short I/O Address Space

A.2.2 **Standardized Module I/O Map**

I/O Interface Block
This 1 Kbyte block of short I/O addresses allocated to each XVME module is mapped with a standardized format to simplify programming and data access. The locations of frequently used registers and module-specific identification information are uniform. For example, the module identification is always found in the first 32 odd bytes of the module memory block -- with these addresses being relative to the jumpered base address (i.e., module I.D. data address = base address + odd bytes 1H - 3FH). The byte located at base address +81H on each module contains a status/control register which provides the results of diagnostics for verification of the module's operational condition.

Module-Specific
The next area of the module I/O interface block (base address + 82H - up to FFFH is module-specific and varies in size from one module to the next. It is in this area that the module holds specific I/O status, data, and pointer registers for use with IPC protocol. All intelligent XVME-I/O modules have an area of their I/O Interface Blocks defined as dual access RAM. This area of memory provides the space where XVME slave I/O modules access their command blocks and where XVME master modules could access their command blocks (i.e., master modules can also access global system memory).

The remainder of the I/O interface block is then allocated to various module-specific tasks, registers, buffers, ports, etc.

Figure A-2 shows an address map of an XVME I/O module interface block, and how it relates to the VMEbus short I/O address space. Notice that any location in the I/O Interface Block may be accessed by simply using the **address formula**:

Module Base Address + Relative Offset = Desired Location

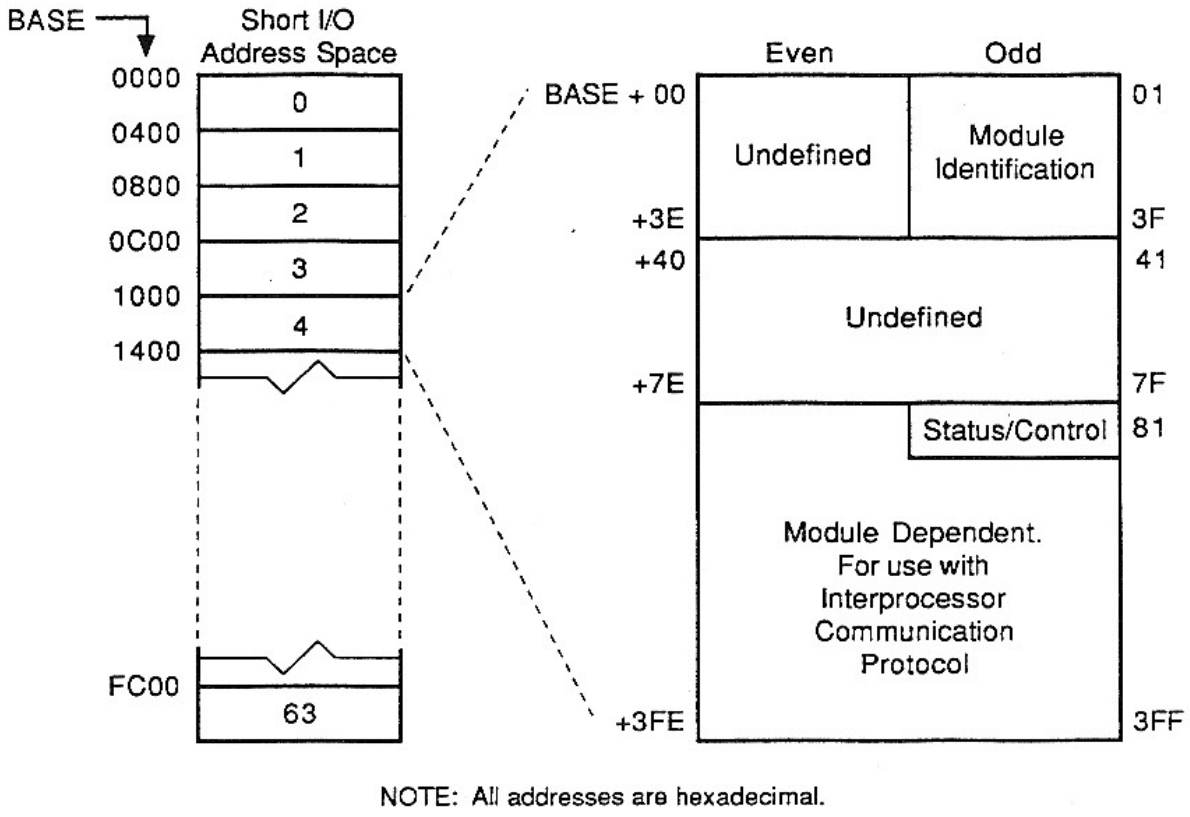


Figure A-2. XVME-I/O Module Address Map

A.3 MODULE SPECIFIC IDENTIFICATION DATA

The module identification scheme provides a unique method of registering module specific information in an ASCII encoded format. The I.D. data is provided as thirty-two ASCII encoded characters consisting of the board type, manufacturer identification, module model number, number of 1 Kbyte blocks occupied by the module, and module functional revision level information. this information can be studied by the system processor on power-up to verify the system configuration and operational status. Table A-1, on the following page, defines the identification information locations.

Table A-1. Module I.D. Data

Offset Relative to Module Base	Contents	ASCII Encoding in Hex	Descriptions
1	V	56	ID PROM identifier, always "VMEID" (5 characters)
3	M	4D	
5	E	45	
7	I	49	
9	D	44	
B	X	58	Manufacturer's I.D.
D	Y	59	
F	C	43	Modules (3 characters)
11	5	35	Module model number (4 characters and 3 trailing blanks)
13	3	33	
15	1	31	
17	*1, 2	31, 32	
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1 Kbyte blocks of I/O space occupied by this module (1 character)
21		20	Major functional revision level with leading blank (if single digit)
23	1	31	
25	1	30	Minor functional revision level with trailing blank (if single digit)
27		20	
29	Undefined	00	Manufacturer-dependent information, reserved for future use
2B	Undefined	00	
2D	Undefined	00	
2F	Undefined	00	
31	Undefined	00	
33	Undefined	00	
35	Undefined	00	
37	Undefined	00	
39	Undefined	00	
3B	Undefined	00	
3D	Undefined	00	
3F	Undefined	00	

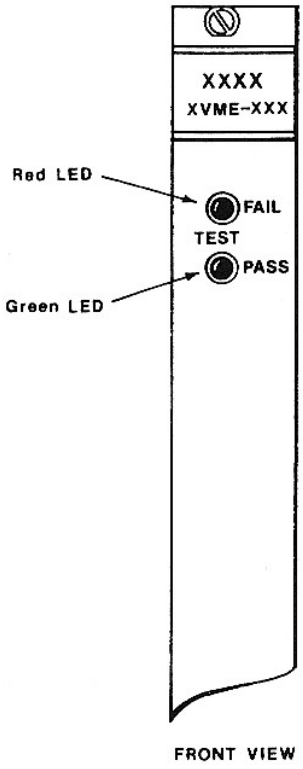
* 1 if 531/1, 2 if 531/2

The module has been designed so that it is only necessary to use odd backplane addresses to access the I.D. data. Thus, each of the 32 bytes of ASCII data have been assigned to the first 32 odd I/O Interface Block bytes (i.e., odd bytes 1 H-3FH).

I.D. Information

I.D. information can be accessed simply by addressing the module base, offset by the specific address for the character(s) needed. For example, if the base address of the board is jumpered to 1000H,and if you wish to access the module model number (I/O interface block locations 11H, 13H, 15H, 17H, 19H, 1BH, and 1DH), you will individually add the offset addresses to the base addresses to read the hex-coded ASCII value at each location. In this example, the ASCII values which make up the module model number are found sequentially at locations 1011H, 1013H, 1015H, 1017H, 1019H, 101BH, and 101DH within the system's short I/O address space.

Figure A-3 shows the location of the status LEDs on the module front panel . The two tables included with Figure A-3 define the visible LED states for the module test conditions on both the intelligent I/O modules and the non-intelligent I/O modules.



Status Bits 3	2	1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	0	0	OFF	ON	ON	Module not yet tested
1	0	0	0	OFF	ON	ON	Module failed test
0	0	0	1	OFF	OFF	OFF	Inactive module
0	1	1	0	ON	ON	ON	Module undergoing test
1	1	1	1	ON	OFF	OFF	Module passed test
all others				X	X	X	Invalid and undefined

INTELLIGENT MODULE STATUS

Status Bits 1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	OFF	ON	ON	Module failed, or not yet tested
0	1	OFF	OFF	OFF	Inactive module
1	0	ON	ON	ON	Module undergoing test
1	1	ON	OFF	OFF	Module passed test

NON-INTELLIGENT MODULE STATUS

Figure A-3. Module LED Status

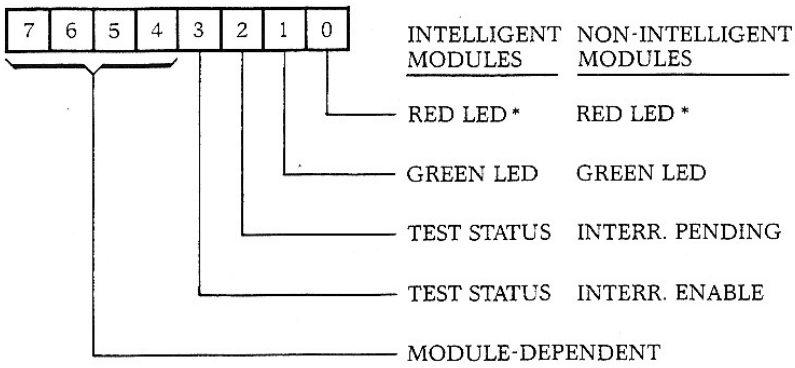
Intelligent Modules

The module status/control register (found at module base address + 81H) on intelligent XVME I/O modules provides the current status of the module self-test in conjunction with the current status of the front panel LEDs. The status register on intelligent modules is a read only register and it can be read by software to determine if the board is operating properly.

Non-Intelligent Modules

On non-intelligent XVME I/O modules, the status/control register is used to indicate the state of the front panel LEDs, and to set and verify module-generated interrupts. The LED status bits are read/write locations which provide the user with the indicators to accommodate diagnostic software. The Interrupt Enable bit is also a read/write location which must be written to in order to enable module-generated interrupts. The Interrupt Pending bit is a read only bit which indicates a module-generate depending interrupt.

Figure A-4 shows the status/control register bit definitions for both intelligent and non-intelligent XVME I/O modules.



Bit	Non-Intelligent Modules	Bit	Intelligent Modules
0	Read/Write - Red LED 0 = Red LED On 1 = Red LED Off	0	Read Only - Red LED 0 = Red LED On 1 = Red LED Off
1	Read/Write - Green LED 0 = Green LED Off 1 = Green LED On	1	Read Only - Green LED 0 = Green LED Off 1 = Green LED On
2	Read Only - Interrupt Pending 0 = No Interrupt 1 = Interrupt Pending	2 & 3	Read Only - Test Status Indicators Bit 3 Bit 2 0 0 = Self-test not started 0 1 = Self-test in progress 1 0 = Self-test failed 1 1 = Self-test passed
3	Read/Write - Interrupt Enable 0 = Interrupts Not Enabled 1 = Interrupts Enabled		
4-7	Module dependent	4-7	Module dependent

Figure A-4. Status Register Bit Definitions

A.5 INTERRUPT CONTROL

Non-Intelligent Modules
Interrupts for non-intelligent modules can be enabled or disabled by setting/clearing the Interrupt Enable bit in the module status register. The status pending on-board interrupts can also be read from this register.

Intelligent Modules
Interrupt control for intelligent modules is handled by the Interprocessor Communications Protocol (IPC).

Appendix B - **VMEbus CONNECTOR/PIN DESCRIPTIONS**

B.1 **INTRODUCTION**

The XVME-531 output module is a double-high (6U) VMEbus compatible module. On the rear edge of the board is a 96-pin bus connector labeled P1. The signals carried by connector P1 are the standard address, data, and control signals required for a P1 backplane interface, as defined by the VMEbus specification. Table B-1, on the following pages, identifies and defines the signals carried by the P1 connector.

Table B-1. VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	1B:3	AC FAILURE: Open-collector driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	1A:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AM0-AM5	1A:23 1B:16,17 18,19 1C:1	ADDRESS MODIFIER (bits 0-5): Three-state driven lines that provide additional information about the address bus, such as: size, cycle type, and/or DTB master identification. ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.
AS*	1A:18	ADDRESS BUS (bits 1-23): Three-state driven address lines that specify a memory address.
A01-A23	1A:24-30 1C:15-30	ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.
A24-A31	2B:4-11	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BBSY*	1B:1	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the DTB master if a higher level is requesting the bus.
BCLR	1B:2	

Table B-1. VMEbus Signal Identification (Continued)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
BERR*	1C11:11	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN* BG3IN*	1B:4,6, 8,10	BUS GRANT (0-3) IN: Totem-pole driven dignals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BGOUT* - BG3OUT*	1B:5,7 9,11	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by Requesters. These signals indicate that a DTB master in the dailsy-chain requires access to the bus.
BR0*-BR3*	1B:12-15	BUS REQUEST (0-3): Open-collector driven signals generated by Requesters. These signals indicate that DTB master in the daisy-chain requires access to the bus.
DS0*	1A:13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur ondata bus lines (D00-D07)
DS1*	1A:12	DATA STROBE 1: Three-state driven signal that indicates druing byte and word transfers that a data transfer will occur on data bus lines (D0-D15).
DTACK*	1A:16	DATA TRANSFER ACKNOWLEDGE: Open collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	1A:1-8 1C:1-8	DATA BUS (bits 0-15): Three-state driven, bi-directional data lines that provide a data path between the DTB master and slave.
GND	1A:9,11 15,17,19 1B:20,23, 1C:9 2B:2,12,22,31	GROUND

Table B-1. VMEbus Signal Identification (Continued)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
IACK*	1A:20	DATA TRANSFER ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot 1 IACKIN* in order to start the interrupt acknowledge daisy-chain.
IRQ1* IRQ7*	1B:24-30	INTERRUPT REQUEST (1-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven in the highest priority.
LWORD*	1C:13	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERVED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	1B:21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B:22	A reserved signal which will be used as the transmission line for serial communication bus messages.
SYSCLK	1A:10	SYSTEM CLOCK: A constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.
SYSFAIL*	1C:10	SYSTEM FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	1C:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	1A:14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation, a low level indicates a write operation.

Table B-1. VMEbus Signal Identification (Continued)

Signal Mnemonic	**Connector and Pin Number**	**Signal Name and Description**
+5V STDBY	1B:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5V	1A:32 1B:32 1C:32 2B:1,13,32	+5 VDC POWER: Used by system logic circuits.
+12V	1C:31	+12 VDC POWER: Used by system logic circuits.
-12V	1A:31	-12 VDC POWER: Used by system logic circuits

BACKPLANE CONNECTOR P1

The following table lists the P1 pin assignments by pin number order. (The connector consists of three rows of pins labeled A, B, and C.)

Table B-2. P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5v STDBY	+12V
32	+5V	+5v	+5v

BACKPLANE CONNECTOR P2

The following table lists the P2 pin assignments by pin number order. (The connector consists of three rows of pins labeled A, B, and C.)

Table B-3. P2 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	User I/O	+5V	User I/O
2	User I/O	GND	User I/O
3	User I/O	Reserved	User I/O
4	User I/O	A24	User I/O
5	User I/O	A25	User I/O
6	User I/O	A26	User I/O
7	User I/O	A27	User I/O
8	User I/O	A28	User I/O
9	User I/O	A29	User I/O
10	User I/O	A30	User I/O
11	User I/O	A31	User I/O
12	User I/O	GND	User I/O
13	User I/O	+5V	User I/O
14	User I/O	D16	User I/O
15	User I/O	D17	User I/O
16	User I/O	D18	User I/O
17	User I/O	D19	User I/O
18	User I/O	D20	User I/O
19	User I/O	D21	User I/O
20	User I/O	D22	User I/O
21	User I/O	D23	User I/O
22	User I/O	GND	User I/O
23	User I/O	D24	User I/O
24	User I/O	D25	User I/O
25	User I/O	D26	User I/O
26	User I/O	D27	User I/O
27	User I/O	D28	User I/O
28	User I/O	D29	User I/O
29	User I/O	D30	User I/O
30	User I/O	D31	User I/O
31	User I/O	GND	User I/O
32	User I/O	+5V	User I/O

Table B-4. Output Connectors P3 and P4

P4 Connector		**P3 Connector**	
Pin	**Definition**	**Pin**	**Definition**
1, 5, 9, 13, 17, 21, 25, 29, 33, 34	AGND	1, 5, 9, 13, 17, 21, 25, 29, 33, 34	AGND
2	VOUT CHAN 0	2	VOUT CHAN 8
3	-IOUT CHAN 0	3	-IOUT CHAN 8
4	+IOUT CHAN 0	4	+IOUT CHAN 8
6	VOUT CHAN 1	6	VOUT CHAN 9
7	-IOUT CHAN 1	7	-IOUT CHAN 9
8	+IOUT CHAN 1	8	+IOUT CHAN 9
10	VOUT CHAN 2	10	VOUT CHAN 10
11	-IOUT CHAN 2	11	-IOUT CHAN 10
12	+IOUT CHAN 2	12	+IOUT CHAN 10
14	VOUT CHAN 3	14	VOUT CHAN 11
15	-IOUT CHAN 3	15	-IOUT CHAN 11
16	+IOUT CHAN 3	16	+IOUT CHAN 11
18	VOUT CHAN 4	18	VOUT CHAN 12
19	-IOUT CHAN 4	19	-IOUT CHAN 12
20	+IOUT CHAN 4	20	+IOUT CHAN 12
22	VOUT CHAN 5	22	VOUT CHAN 13
23	-IOUT CHAN 5	23	-IOUT CHAN 13
24	+IOUT CHAN 5	24	+IOUT CHAN 13
26	VOUT CHAN 6	26	VOUT CHAN 14
27	-IOUT CHAN 6	27	-IOUT CHAN 14
28	+IOUT CHAN 6	28	+IOUT CHAN 14
30	VOUT CHAN 7	30	VOUT CHAN 15
31	-IOUT CHAN 7	31	-IOUT CHAN 15
32	+IOUT CHAN 7	32	+IOUT CHAN 15

Appendix C - **QUICK REFERENCE GUIDE**

This appendix contains the following contents for easy reference:

- Memory Map
- Jumper Listings
- Switch Options
- Jumper Options
- Connector Pinout
- Register Definitions
- Unipolar and Bipolar Mode Formats
- D/A Reset
- Calibration POTS
- Calibration Points

	Even	Odd	
Base +00H 3EH			01H 3FH
	Undefined	Identification	
40H 7EH	Reserved	Reserved	41H 7FH
80H	Undefined	Status/Control	81H
82H 86H	Undefined	Undefined	83H 87H
88H	Channel 0 D/A High	Channel 0 D/A Low	89H
8AH	Channel 1 D/A High	Channel 1 D/A Low	8BH
8CH	Channel 2 D/A High	Channel 2 D/A Low	8DH
8EH	Channel 3 D/A High	Channel 3 D/A Low	8FH
90H	Channel 4 D/A High	Channel 4 D/A Low	91H
92H	Channel 5 D/A High	Channel 5 D/A Low	93H
94H	Channel 6 D/A High	Channel 6 D/A Low	95H
96H	Channel 7 D/A High	Channel 7 D/A Low	97H
98H	Channel 8 D/A High	Channel 8 D/A Low	99H
9AH	Channel 9 D/A High	Channel 9 D/A Low	9BH
9CH	Channel 10 D/A High	Channel 10 D/A Low	9DH
9EH	Channel 11 D/A High	Channel 11 D/A Low	9FH
A0H	Channel 12 D/A High	Channel 12 D/A Low	A1H
A2H	Channel 13 D/A High	Channel 13 D/A Low	A3H
A4H	Channel 14 D/A High	Channel 14 D/A Low	A5H
A6H	Channel 15 D/A High	Channel 15 D/A Low	A7H
A8H C6H	Reserved		A9H C7H
C8H E6H			C9H E7H
E8H	Channel 0-15 Update Register		E9H
EAH FEH			EBH FFH
	Reserved		

Figure C-1. XVME-531 Memory Map

Table C-1. Jumper Listing

Jumper	Function
J1	SYSFAIL jumper
J2	Selects straight/offset binary or two's compliment for channel 14
J3	Selects straight/offset binary or two's compliment for channel 12
J4	Selects straight/offset binary or two's compliment for channel 10
J5	Selects straight/offset binary or two's compliment for channel 8
J6	Selects straight/offset binary or two's compliment for channel 6
J7	Selects straight/offset binary or two's compliment for channel 4
J8	Selects straight/offset binary or two's compliment for channel 2
J9	Selects straight/offset binary or two's compliment for channel 0
J10	Used to select Unipolar or Bipolar operation for channel 15
J11	Used to select Unipolar or Bipolar operation for channel 14
J12	Used to select Unipolar or Bipolar operation for channel 13
J13	Used to select Unipolar or Bipolar operation for channel 12
J14	Used to select Unipolar or Bipolar operation for channel 11
J15	Used to select Unipolar or Bipolar operation for channel 10
J16	Used to select Unipolar or Bipolar operation for channel 9
J17	Used to select Unipolar or Bipolar operation for channel 8
J18	Used to select Unipolar or Bipolar operation for channel 7
J19	Used to select Unipolar or Bipolar operation for channel 6
J20	Used to select Unipolar or Bipolar operation for channel 5
J21	Used to select Unipolar or Bipolar operation for channel 4
J22	Used to select Unipolar or Bipolar operation for channel 3
J23	Used to select Unipolar or Bipolar operation for channel 2
J24	Used to select Unipolar or Bipolar operation for channel 1
J25	Used to select Unipolar or Bipolar operation for channel 0
J26	Used to select output voltage span for channel 15
J27	Used to select output voltage span for channel 14
J28	Used to select output voltage span for channel 13
J29	Used to select output voltage span for channel 12

Table continued on the following page

Table C-1. Jumper Listing (Continued)

Jumper	Function
J30	Used to select output voltage span for channel 11
J31	Used to select output voltage span for channel 10
J32	Used to select output voltage span for channel 9
J33	Used to select output voltage span for channel 8
J34	Used to select output voltage span for channel 7
J35	Used to select output voltage span for channel 6
J36	Used to select output voltage span for channel 5
J37	Used to select output voltage span for channel 4
J38	Used to select output voltage span for channel 3
J39	Used to select output voltage span for channel 2
J40	Used to select output voltage span for channel 1
J41	Used to select output voltage span for channel 0
J42	Select straight/offset binary or two's compliment for channel 15
J43	Select straight/offset binary or two's compliment for channel 13
J44	Select straight/offset binary or two's compliment for channel 11
J45	Select straight/offset binary or two's compliment for channel 9
J46	Select straight/offset binary or two's compliment for channel 7
J47	Select straight/offset binary or two's compliment for channel 5
J48	Select straight/offset binary or two's compliment for channel 3
J49	Select straight/offset binary or two's compliment for channel 1
J50*	Used to select voltage or current mode for channel 15
J51*	Used to select voltage or current mode for channel 14
J52*	Used to select voltage or current mode for channel 13
J53*	Used to select voltage or current mode for channel 12
J54*	Used to select voltage or current mode for channel 11
J55*	Used to select voltage or current mode for channel 10
J56*	Used to select voltage or current mode for channel 9
J57*	Used to select voltage or current mode for channel 8
J58*	Used to select voltage or current mode for channel 7
J59*	Used to select voltage or current mode for channel 6
J60*	Used to select voltage or current mode for channel 5
J61*	Used to select voltage or current mode for channel 4
J62*	Used to select voltage or current mode for channel 3
J63*	Used to select voltage or current mode for channel 2
J64*	Used to select voltage or current mode for channel 1
J65*	Used to select voltage or current mode for channel 0

* Used on the 531/2 only

Table C-2. VMEbus Switch Options

VMEbus OPTIONS	
Switch 1	**Used to configure address**
Position 1-6	Module base address select jumpers. Refer to Section 2.5.1.
Position 7	This switch position determines whether the module will respond to only supervisory access or to both supervisory and non-privileged accesses. Refer to Section 2.5.2.
Position 8	This switch position determines whether the module will reside in the short I/O address space or FFXXXX in the standard address space. Refer to Section 2.5.3

Table C-3. Base Address Switch Options Switch 1 Position

Switch 1 Position						BaseAddress of Module
6	5	4	3	2	1	(Hex)
0	0	0	0	0	0	0000
0	0	0	0	0	1	0400
0	0	0	0	1	0	0800
0	0	0	0	1	1	0C00
0	0	0	1	0	0	1000
0	0	0	1	0	1	1400
0	0	0	1	1	0	1800
0	0	0	1	1	1	1C00
0	0	1	0	0	0	2000
0	0	1	0	0	1	2400
0	0	1	0	1	0	2800
0	0	1	0	1	1	2C00
0	0	1	1	0	0	3000
0	0	1	1	0	1	3400
0	0	1	1	1	0	3800
0	0	1	1	1	1	3C00
0	1	0	0	0	0	4000
0	1	0	0	0	1	4400
0	1	0	0	1	0	4800
0	1	0	0	1	1	4C00
0	1	0	1	0	0	5000
0	1	0	1	0	1	5400
0	1	0	1	1	0	5800
0	1	0	1	1	1	5C00
0	1	1	0	0	0	6000
0	1	1	0	0	1	6400
0	1	1	0	1	0	6800
0	1	1	0	1	1	6C00
0	1	1	1	0	0	7000
0	1	1	1	0	1	7400
0	1	1	1	1	0	7800
0	1	1	1	1	1	7C00
1	0	0	0	0	0	8000
1	0	0	0	0	1	8400
1	0	0	0	1	0	8800
1	0	0	0	1	1	8C00
1	0	0	1	0	0	9000
1	0	0	1	0	1	9400
1	0	0	1	1	0	9800
1	0	0	1	1	1	9C00
1	0	1	0	0	0	A000
1	0	1	0	0	1	A400
1	0	1	0	1	0	A800
1	0	1	0	1	1	AC00

Open = Logic "1"
Closed = Logic "0"

(Table continued on the following page)

Table C-3. Base Address Settings Switch 1 (Continued)

Switch 1 Position						**Base Address** of Module
6	5	4	3	2	1	(Hex)
1	0	1	1	0	0	B000
1	0	1	1	0	1	B400
1	0	1	1	1	0	B800
1	0	1	1	1	1	BC00
1	1	0	0	0	0	C000
1	1	0	0	0	1	C400
1	1	0	0	1	0	C800
1	1	0	0	1	1	CC00
1	1	0	1	0	0	D000
1	1	0	1	0	1	D400
1	1	0	1	1	0	D800
1	1	0	1	1	1	DC00
1	1	1	0	0	0	E000
1	1	1	0	0	1	E400
1	1	1	0	1	0	E800
1	1	1	0	1	1	EC00
1	1	1	1	0	0	F000
1	1	1	1	0	1	F400
1	1	1	1	1	0	F800
1	1	1	1	1	1	FC00

Open = Logic "1"
Closed = Logic "0"

Table C-4. Address Modifier Code Options

Address Space	**Switch 1**		**Address Modifier Code**	**Access Mode**
	Pos 7	**Pos 8**		
Short I/O	Open	Closed	2DH only	Supervisory Only
	Closed	Closed	29H and 2DH	Supervisory or Non-privileged
Standard	Open	Open	3DH only	Supervisory Only
	Closed	Open	39H and 3DH	Supervisory or Non-privileged

Table C-5. Digital to Analog Conversion Jumper Options

DIGITAL TO ANALOG CONVERSION OPTIONS	
Jumper	**Use**
J2 - J9, and J42 - J49	These jumpers provide the option to individually configure each output channel to convert either straight binary to analog or to convert two's complement binary to analog. Refer to Section 2.6.1
J10 - J41	These groups of jumpers select one of three output voltage ranges for each output channel. One of these jumpers also activate calibration potentiometers (specific to each channel) to provide for the adjustment of either unipolar offset or for the adjustment of bipolar offset voltage. Refer to Section 2.6.2
J50 - J65	On the XVME-531/2 only, these jumpers configure the 16 output channels to convert data to either an analog voltage format or an analog current format. Refer to Section 2.6.3.

Table C-6. Output Conversion Format Jumpers

Output Channel	Digital Data Conversion Formats	
	Straight/Offset Binary	**Two's Complement**
0	J9A	J9B
1	J49A	J49B
2	J8A	J8B
3	J48A	J48B
4	J7A	J7B
5	J47A	J47B
6	J6A	J6B
7	J46A	J46B
8	J5A	J5B
9	J45A	J45B
10	J4A	J4B
11	J44A	J44B
12	J3A	J3B
13	J43A	J43B
14	J2A	J2B
15	J42A	J42B

Table C-7. Output Voltage Range Configurations

Channel	Jumper	Output Voltage Ranges		
		0 - 10V	**±5V**	**±10V**
0	J25 J41	B B	A B	A A
1	J24 J40	B B	A B	A A
2	J23 J39	B B	A B	A A
3	J22 J38	B B	A B	A A
4	J21 J37	B B	A B	A A
5	J20 J36	B B	A B	A A
6	J19 J35	B B	A B	A A
7	J18 J34	B B	A B	A A
8	J17 J33	B B	A B	A A
9	J16 J32	B B	A B	A A
10	J15 J31	B B	A B	A A
11	J14 J30	B B	A B	A A
12	J13 J29	B B	A B	A A
13	J12 J28	B B	A B	A A
14	J11 J27	B B	A B	A A
15	J10 J26	B B	A B	A A

Table C-8. Voltage/Current Output Selection Jumpers
(XVME-531/2 Option Only)

Output Channel	Output	
	Voltage	**Current**
0	J65A	J65B
1	J64A	J64B
2	J63A	J63B
3	J62A	J62B
4	J61A	J61B
5	J60A	J60B
6	J59A	J59B
7	J58A	J58B
8	J57A	J57B
9	J56A	J56B
10	J55A	J55B
11	J54A	J54B
12	J53A	J53B
13	J52A	J52B
14	J51A	J51B
15	J50A	J50B

Refer to Section 2.6.3

Table C-9. Output Connectors P3 and P4

P4 Connector		**P3 Connector**	
Pin	**Definition**	**Pin**	**Definition**
1, 5, 9, 13, 17, 21, 25, 29, 33, 34	AGND	1, 5, 9, 13, 17, 21, 25, 29, 33, 34	AGND
2	VOUT CHAN 0	2	VOUT CHAN 8
3	-IOUT CHAN 0	3	-IOUT CHAN 8
4	+IOUT CHAN 0	4	+IOUT CHAN 8
6	VOUT CHAN 1	6	VOUT CHAN 9
7	-IOUT CHAN 1	7	-IOUT CHAN 9
8	+IOUT CHAN 1	8	+IOUT CHAN 9
10	VOUT CHAN 2	10	VOUT CHAN 10
11	-IOUT CHAN 2	11	-IOUT CHAN 10
12	+IOUT CHAN 2	12	+IOUT CHAN 10
14	VOUT CHAN 3	14	VOUT CHAN 11
15	-IOUT CHAN 3	15	-IOUT CHAN 11
16	+IOUT CHAN 3	16	+IOUT CHAN 11
18	VOUT CHAN 4	18	VOUT CHAN 12
19	-IOUT CHAN 4	19	-IOUT CHAN 12
20	+IOUT CHAN 4	20	+IOUT CHAN 12
22	VOUT CHAN 5	22	VOUT CHAN 13
23	-IOUT CHAN 5	23	-IOUT CHAN 13
24	+IOUT CHAN 5	24	+IOUT CHAN 13
26	VOUT CHAN 6	26	VOUT CHAN 14
27	-IOUT CHAN 6	27	-IOUT CHAN 14
28	+IOUT CHAN 6	28	+IOUT CHAN 14
30	VOUT CHAN 7	30	VOUT CHAN 15
31	-IOUT CHAN 7	31	-IOUT CHAN 15
32	+IOUT CHAN 7	32	+IOUT CHAN 15

Table C-10. Module I.D. Data

Offset Relative to Module Base	Contents	ASCII Encoding in Hex	Descriptions
1	V	56	ID PROM identifier, always "VMEID" (5 characters)
3	M	4D	
5	E	45	
7	I	49	
9	D	44	
B	X	58	Manufacturer's I.D.
D	Y	59	
F	C	43	Modules (3 characters)
11	5	35	Module model number (4 characters and 3 trailing blanks)
13	3	33	
15	1	31	
17	*1, 2	31, 32	
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1 Kbyte blocks of I/O space occupied by this module (1 character)
21		20	Major functional revision level with leading blank (if single digit)
23	1	31	
25	1	30	Minor functional revision level with trailing blank (if single digit)
27		20	
29	Undefined	00	Manufacturer-dependent information, reserved for future use
2B	Undefined	00	
2D	Undefined	00	
2F	Undefined	00	
31	Undefined	00	
33	Undefined	00	
35	Undefined	00	
37	Undefined	00	
39	Undefined	00	
3B	Undefined	00	
3D	Undefined	00	
3F	Undefined	00	

* 1 if 531/1, 2 if 531/2

Table C-11. Status/Control Register (Base + 81H)

BIT #	FUNCTION	
	STATUS	**CONTROL**
D0	SYSFAIL (Red LED)	SYSFAIL (Red LED)
D1	PASS (Green LED)	PASS (Green LED)
D2	Not Used	Not Used
D3	Not Used	Not Used
D4	Module Reset	Module Reset
D5	Mode Bit	Mode Bit
D6	Not Used	Not Used
D7	D/A Busy	Not Used

Table C-12. Pass/Fail LEDs

Status **D1**	**Bits** **D0**	**LEDs** **Green**	**Red**	**SYSFAIL***	**Status**
0	0	Off	On	Active**	Module failed or not yet tested
0	1	Off	Off	Inactive	Inactive module
1	0	On	On	Active**	Module under test
1	1	On	Off	Inactive	Module passed test

**SYSFAIL will be active if SYSFAIL enable/disable jumper is set to the enabled position, otherwise it will be inactive. (Refer to Section 2.5.5.)

Table C-13. Update Register/Bit Definition

Address	BIT	CHANNEL	DEFINITION
E9	0	Channel 0 Update Bit	1 = Update Chan 0 = No Update
E9	1	Channel 1 Update Bit	1 = Update Chan 0 = No Update
E9	2	Channel 2 Update Bit	1 = Update Chan 0 = No Update
E9	3	Channel 3 Update Bit	1 = Update Chan 0 = No Update
E9	4	Channel 4 Update Bit	1 = Update Chan 0 = No Update
E9	5	Channel 5 Update Bit	1 = Update Chan 0 = No Update
E9	6	Channel 6 Update Bit	1 = Update Chan 0 = No Update
E9	7	Channel 7 Update Bit	1 = Update Chan 0 = No Update
E8	0	Channel 8 Update Bit	1 = Update Chan 0 = No Update
E8	1	Channel 9 Update Bit	1 = Update Chan 0 = No Update
E8	2	Channel 10 Update Bit	1 = Update Chan 0 = No Update
E8	3	Channel 11 Update Bit	1 = Update Chan 0 = No Update
E8	4	Channel 12 Update Bit	1 = Update Chan 0 = No Update
E8	5	Channel 13 Update Bit	1 = Update Chan 0 = No Update
E8	6	Channel 14 Update Bit	1 = Update Chan 0 = No Update
E8	7	Channel 15 Update Bit	1 = Update Chan 0 = No Update

NOTE
The update register +E8, and +E9 may be written as a byte or word at a time.

Table C-14 Unipolar Mode (Straight Binary Encoding)

X = Don't Care Straight Binary Format Voltage Mode: D_{15} D_0	Analog Output
X X X X 1 1 1 1 1 1 1 1 1 1 1 1 X X X X 1 0 0 0 0 0 0 0 0 0 0 0 X X X X 0 0 0 0 0 0 0 0 0 0 0 0	Vfsr - 1 LSB Vfsr/2 0V
Current Mode (XVME-531/1/2 only): D_{15} D_0	Analog Output 4 - 20mA
X X X X 1 1 1 1 1 1 1 1 1 1 1 1 X X X X 1 0 0 0 0 0 0 0 0 0 0 0 X X X X 0 0 0 0 0 0 0 0 0 0 0 0	19.996mA (20mA - 1 LSB) 12mA 4mA

Table C-15. Bipolar Modes

X = Don't Care Offset Binary Format: D_{15} D_0	Analog Output
X X X X 1 1 1 1 1 1 1 1 1 1 1 1 X X X X 1 1 0 0 0 0 0 0 0 0 0 0 X X X X 1 0 0 0 0 0 0 0 0 0 0 0 X X X X 0 1 0 0 0 0 0 0 0 0 0 0 X X X X 0 0 0 0 0 0 0 0 0 0 0 0	+Vfsr - 1 LSB Vfsr/2 0V -Vfsr/2 -Vfsr
Two's Compliment Format: D_{15} D_0	Analog Output
X X X X 1 1 1 1 1 1 1 1 1 1 1 1 X X X X 0 1 0 0 0 0 0 0 0 0 0 0 X X X X 0 0 0 0 0 0 0 0 0 0 0 0 X X X X 1 1 0 0 0 0 0 0 0 0 0 0 X X X X 1 0 0 0 0 0 0 0 0 0 0 0	+Vfsr - 1 LSB 1/2 (+Vfsr) 0V 1/2 (-Vfsr) -Vfsr

Table C-16. D/A Output Affected

Jumpered For	Digital Reset Value	Analog Reset Value
Unipolar 0-10V straight binary	000H	0V
Unipolar 4-20mA straight binary 531-2	000H	4mA
Bipolar ±5V offset binary	000H	-5V
Bipolar ±5V two's compliment	800H	0V
Bipolar ±10V offset bianry	000H	-10V
Bipolar ±10V two's compliment	800H	0V

Table C-17. D/A Calibration Potentiometers

Resistor	Description
R112 R78 R44	Channel 0 Unipolar Adjustment Channel 0 Bipolar Adjustment Channel 0 Gain Adjustment
R111 R77 R43	Channel 1 Unipolar Adjustment Channel 1 Bipolar Adjustment Channel 1 Gain Adjustment
R110 R76 R42	Channel 2 Unipolar Adjustment Channel 2 Bipolar Adjustment Channel 2 Gain Adjustment
R109 R75 R41	Channel 3 Unipolar Adjustment Channel 3 Bipolar Adjustment Channel 3 Gain Adjustment
R108 R74 R40	Channel 4 Unipolar Adjustment Channel 4 Bipolar Adjustment Channel 4 Gain Adjustment
R107 R73 R39	Channel 5 Unipolar Adjustment Channel 5 Bipolar Adjustment Channel 5 Gain Adjustment
R106 R72 R38	Channel 6 Unipolar Adjustment Channel 6 Bipolar Adjustment Channel 6 Gain Adjustment
R105 R71 R37	Channel 7 Unipolar Adjustment Channel 7 Bipolar Adjustment Channel 7 Gain Adjustment
R104 R70 R36	Channel 8 Unipolar Adjustment Channel 8 Bipolar Adjustment Channel 8 Gain Adjustment
R103 R69 R35	Channel 9 Unipolar Adjustment Channel 9 Bipolar Adjustment Channel 9 Gain Adjustment
R102 R68 R34	Channel 10 Unipolar Adjustment Channel 10 Bipolar Adjustment Channel 10 Gain Adjustment
R101 R67 R33	Channel 11 Unipolar Adjustment Channel 11 Bipolar Adjustment Channel 11 Gain Adjustment

Table C-17. D/A Calibration Potentiometers (Continued)

Resistor	Description
R100 R66 R32	Channel 12 Unipolar Adjustment Channel 12 Bipolar Adjustment Channel 12 Gain Adjustment
R99 R65 R31	Channel 13 Unipolar Adjustment Channel 13 Bipolar Adjustment Channel 13 Gain Adjustment
R98 R64 R30	Channel 14 Unipolar Adjustment Channel 14 Bipolar Adjustment Channel 14 Gain Adjustment
R97 R63 R29	Channel 15 Unipolar Adjustment Channel 15 Bipolar Adjustment Channel 15 Gain Adjustment

Table C-18. D/A -FS Calibration Points

-FS CALIBRATION			
Binary Encoding Mode	**Voltage Range**	**Digital Data In**	**Analog Valve Out (-FS)**
UNIPOLAR (Straight Binary	4-20mA 0-10V	0000H 0000H	4mA 0V
BIPOLAR (Offset Binary)	±5V ±10V	0000H 0000H	-5V -10V
BIPOLAR (Two's Complement)	±5V ±10V	0800H 0800H	-5V -10V

Table C-19. D/A +FS Calibration Points

+FS CALIBRATION			
Binary Encoding Mode	**Voltage Range**	**Digital Data In**	**Analog Voltage Out (+FS - 1 LSB)**
UNIPOLAR (Straight Binary	4-20mA 0-10V	FFFH FFFH	19.9961mA 9.9976V
BIPOLAR (Offset Binary)	±5V ±10V	FFFH FFFH	4.9976V 9.9951V
BIPOLAR (Two's Complement)	±5V ±10V	07FFH 07FFH	4.9976V 9.9951V

Appendix D - **BLOCK DIAGRAM, ASSEMBLY DRAWING, AND SCHEMATICS**

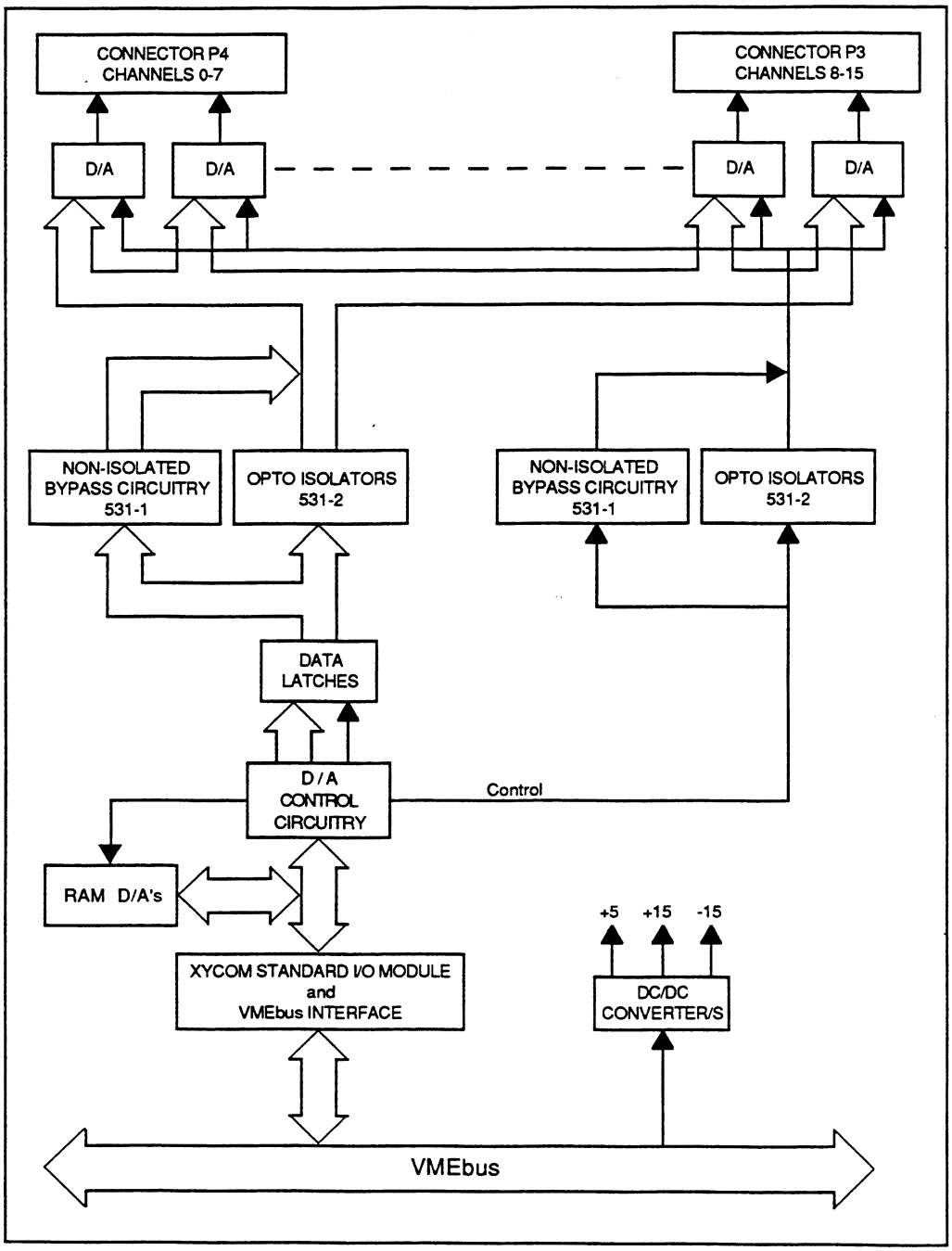


Figure D-1. XVME-531 Block Diagram

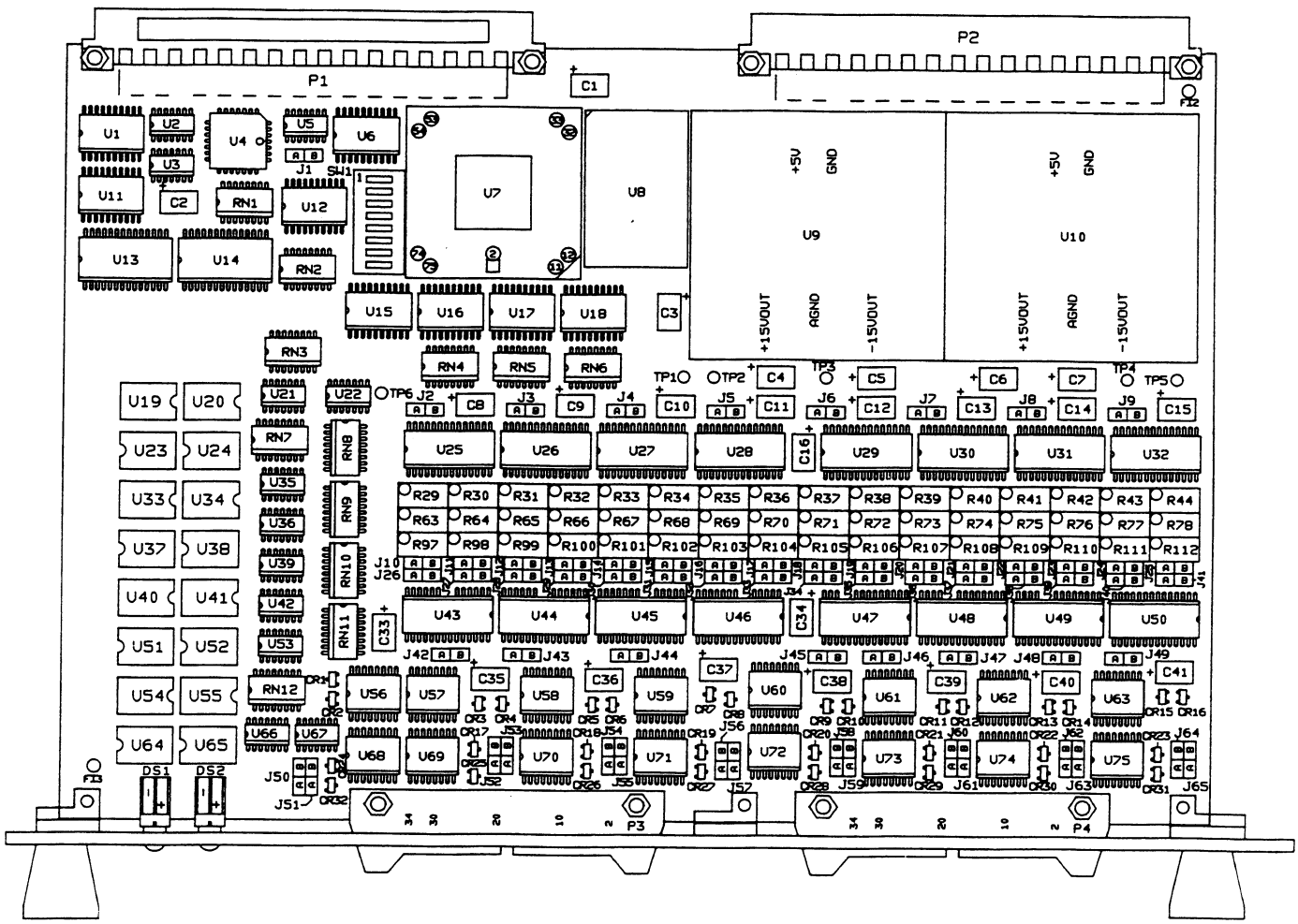
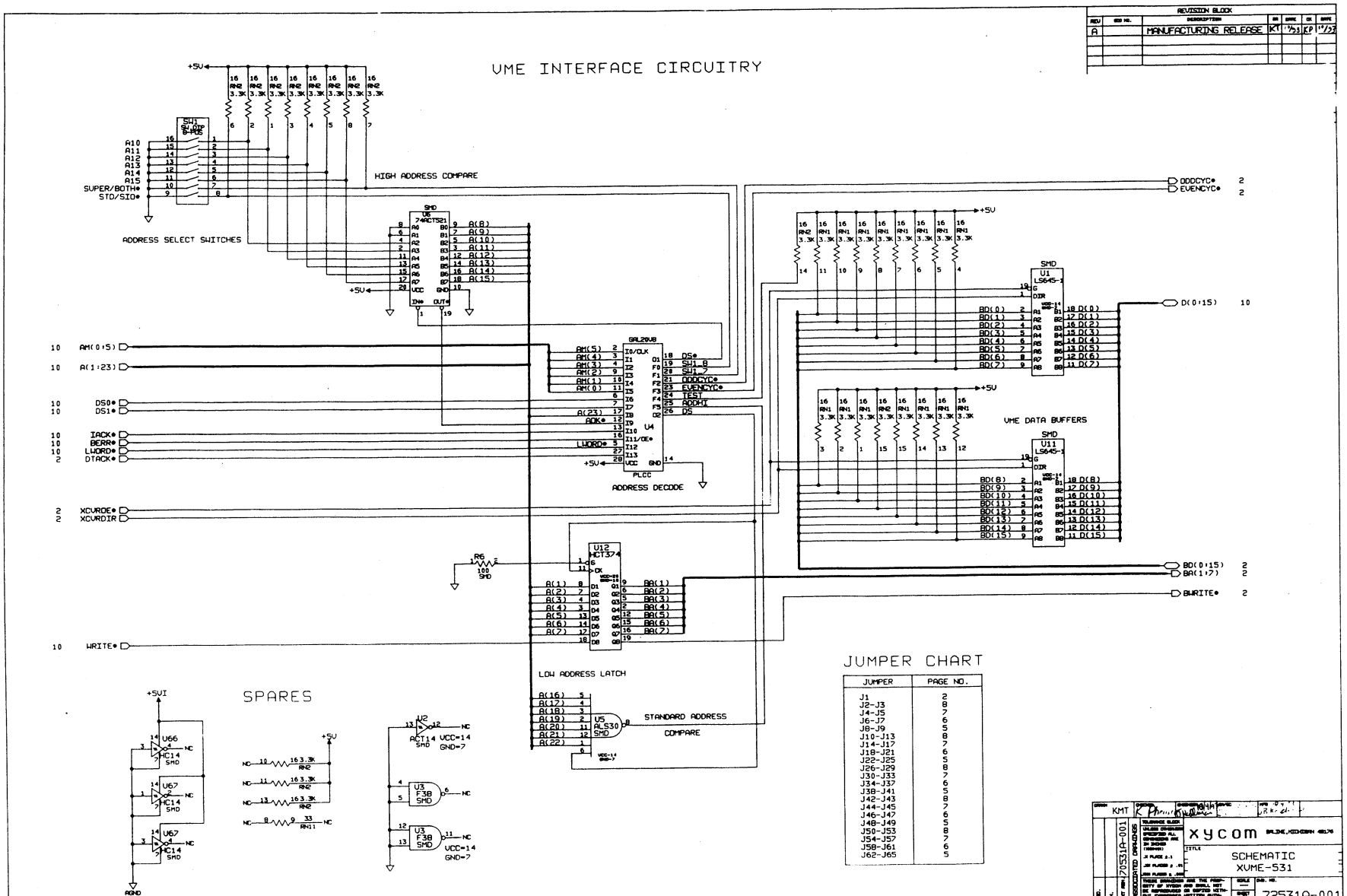
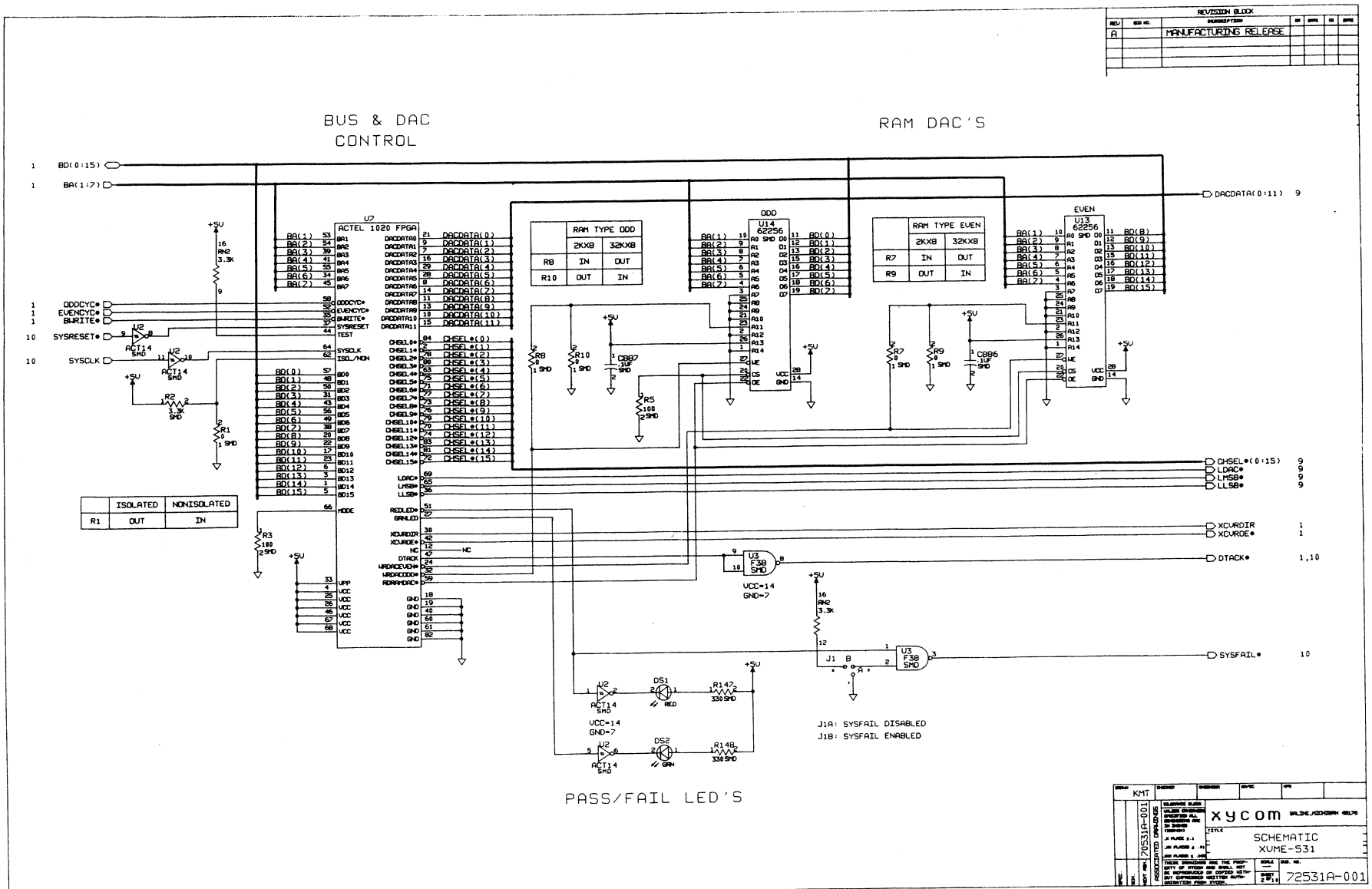


Figure D-2. XVME-531 Assembly Drawing


VME INTERFACE CIRCUITRY
REVISION BLOCK
A
MANUFACTURING RELEASE
HIGH ADDRESS COMPARE
ADDRESS SELECT SWITCHES
SUPER/BOTH*
STD/SIO*
ADDRESS DECODE
VME DATA BUFFERS
LOW ADDRESS LATCH
STANDARD ADDRESS
COMPARE
SPARES
JUMPER CHART
JUMPER
PAGE NO.
J1 2
J2-J3 8
J4-J5 7
J6-J7 6
J8-J9 5
J10-J13 8
J14-J17 7
J18-J21 6
J22-J25 5
J26-J29 8
J30-J33 7
J34-J37 6
J38-J41 5
J42-J43 8
J44-J45 7
J46-J47 6
J48-J49 5
J50-J53 8
J54-J57 7
J58-J61 6
J62-J65 5
xycom
SCHEMATIC
XVME-531
72531A-001



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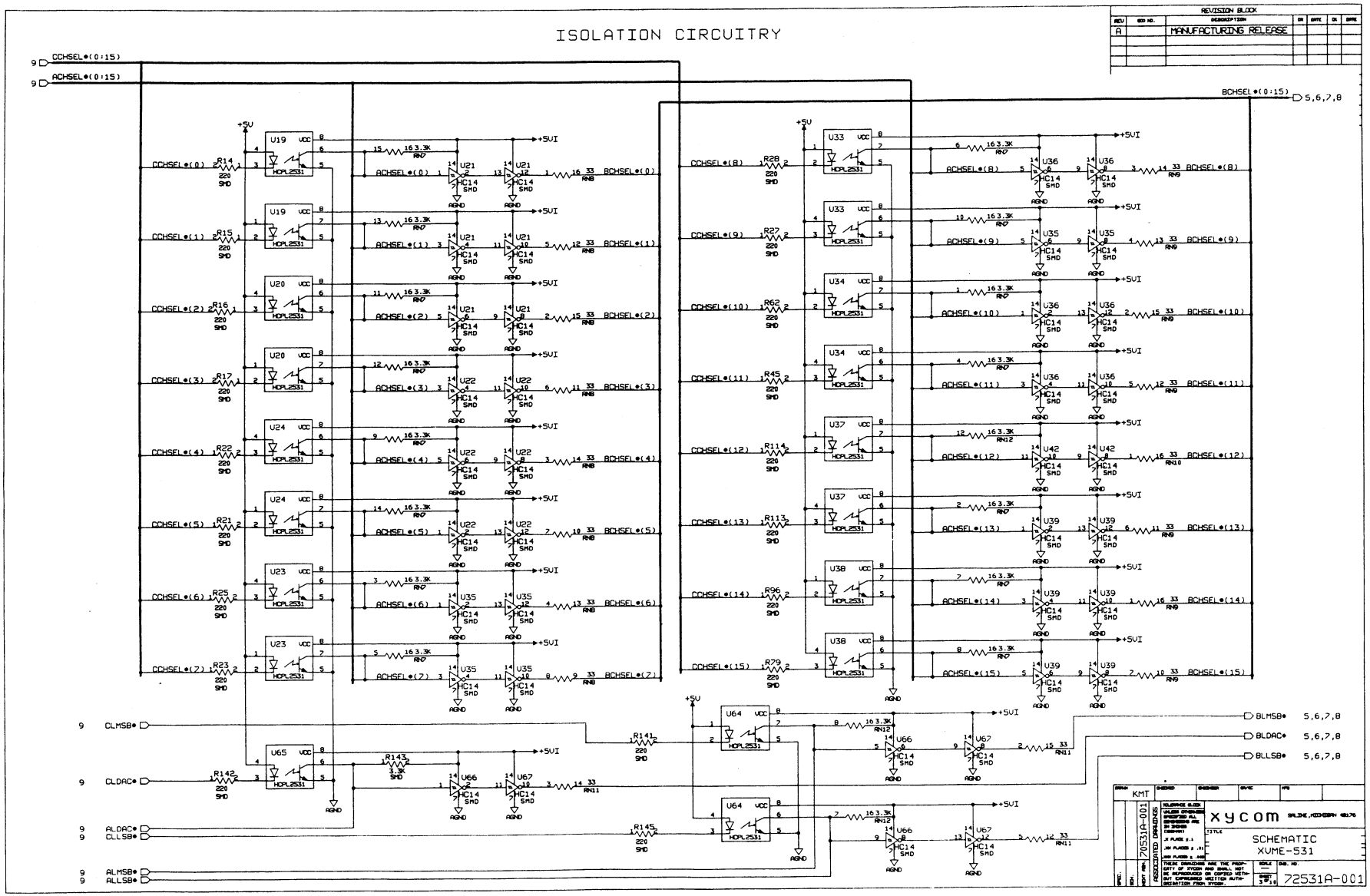
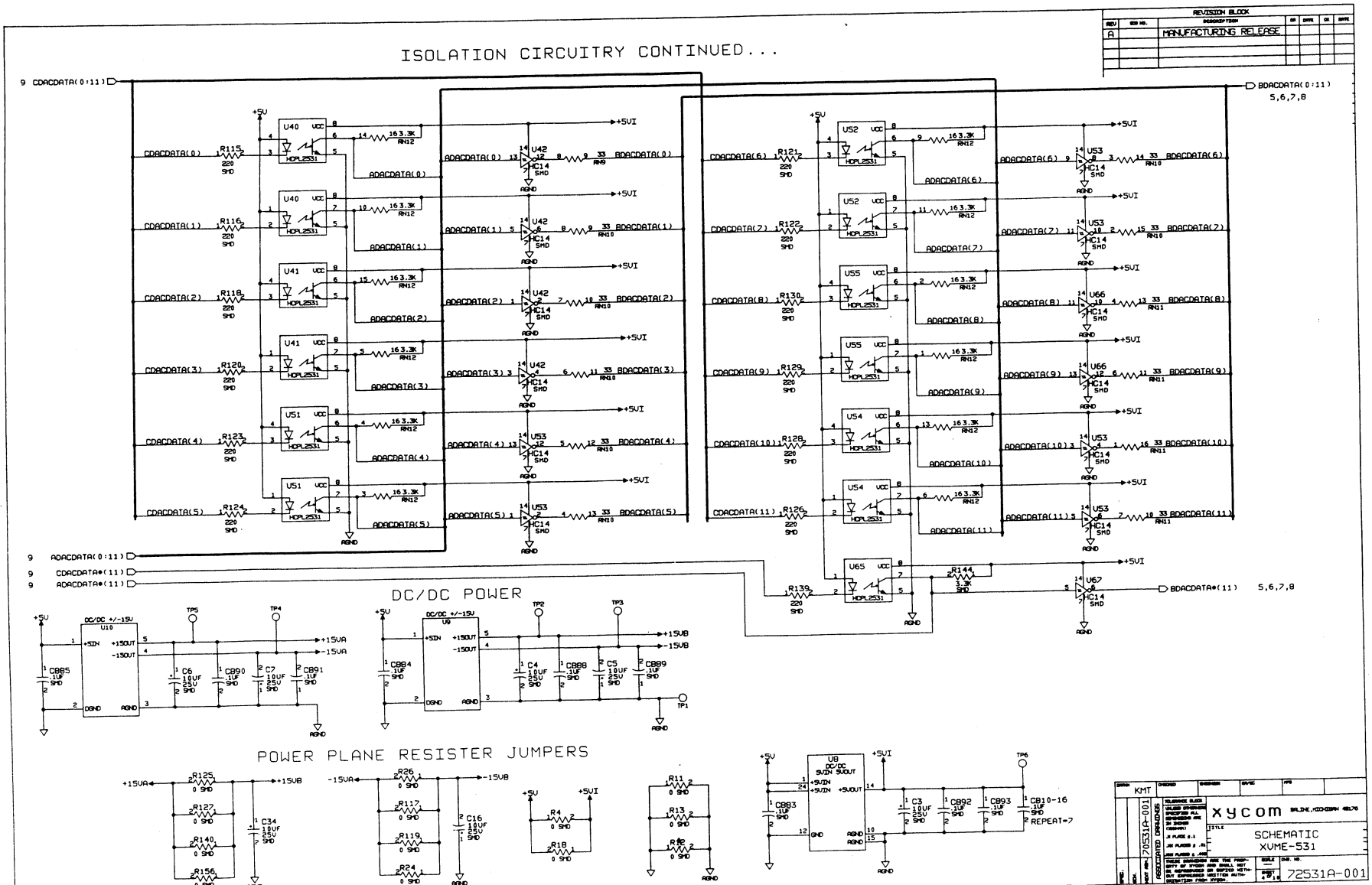
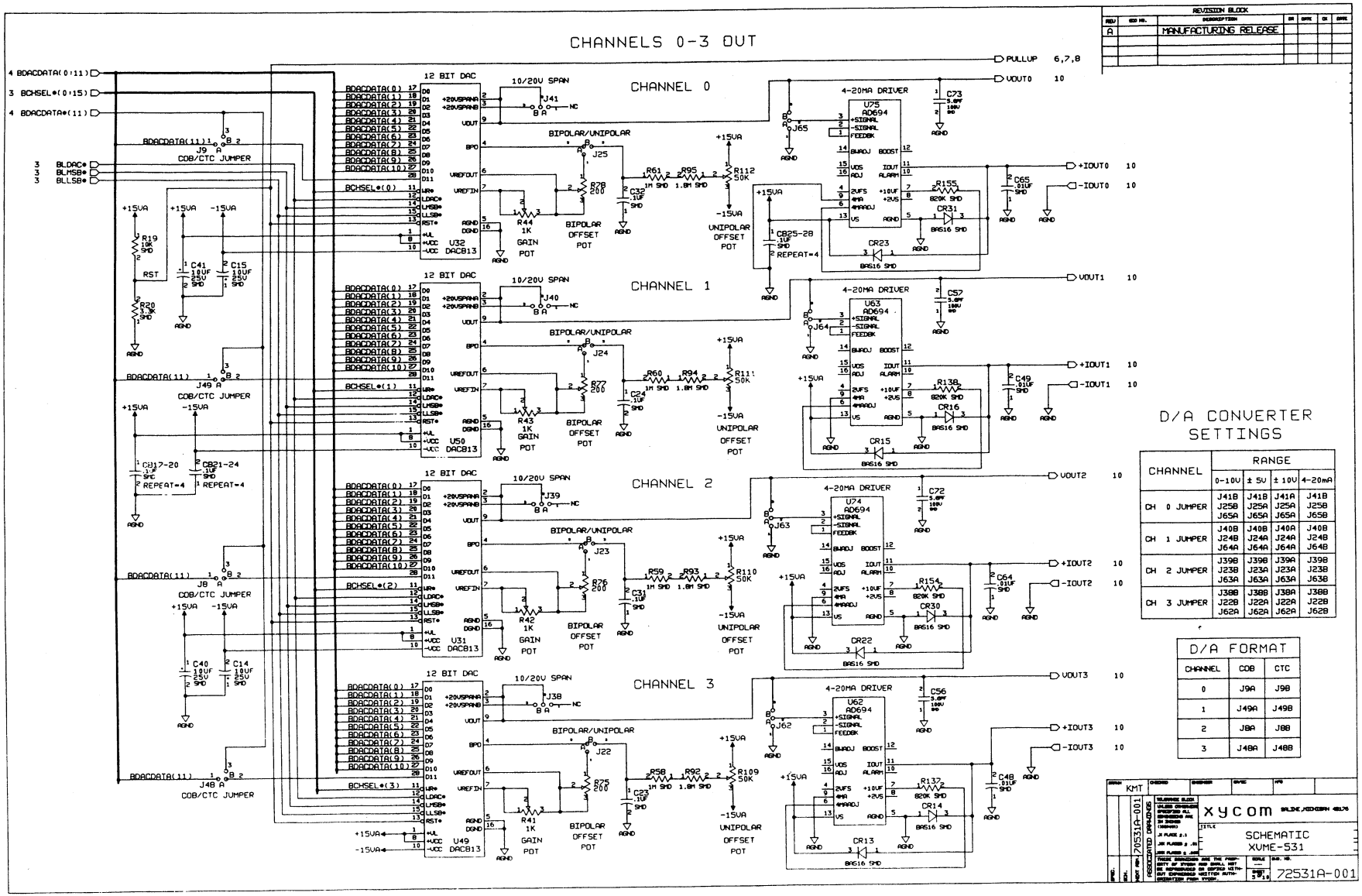

ISOLATION CIRCUITRY
REVISION BLOCK
MANUFACTURING RELEASE
CCHSEL*(0:15)
ACHSEL*(0:15)
BCHSEL*(0:15)
5,6,7,8
+5V
+5VI
AGND
HCPL2531
HC14 SMD
163.3K RN7
163.3K RN12
33 RN8
33 RN9
33 RN10
33 RN11
220 SMD
CLMSB*
CLDAC*
CLLSB*
ALDAC*
ALLSB*
ALMSB*
BLMSB*
BLDAC*
BLLSB*
KMT
xycom
SCHEMATIC
XVME-531
70531A-001
72531A-001


ISOLATION CIRCUITRY CONTINUED...
REVISION BLOCK
A MANUFACTURING RELEASE
9 CDACDATA(0:11)
BDACDATA(0:11)
5,6,7,8
9 ADACDATA(0:11)
9 CDACDATA*(11)
9 ADACDATA*(11)
BDACDATA*(11) 5,6,7,8
DC/DC POWER
POWER PLANE RESISTER JUMPERS
REPEAT=7
KMT
xycom
SCHEMATIC
XVME-531
72531A-001



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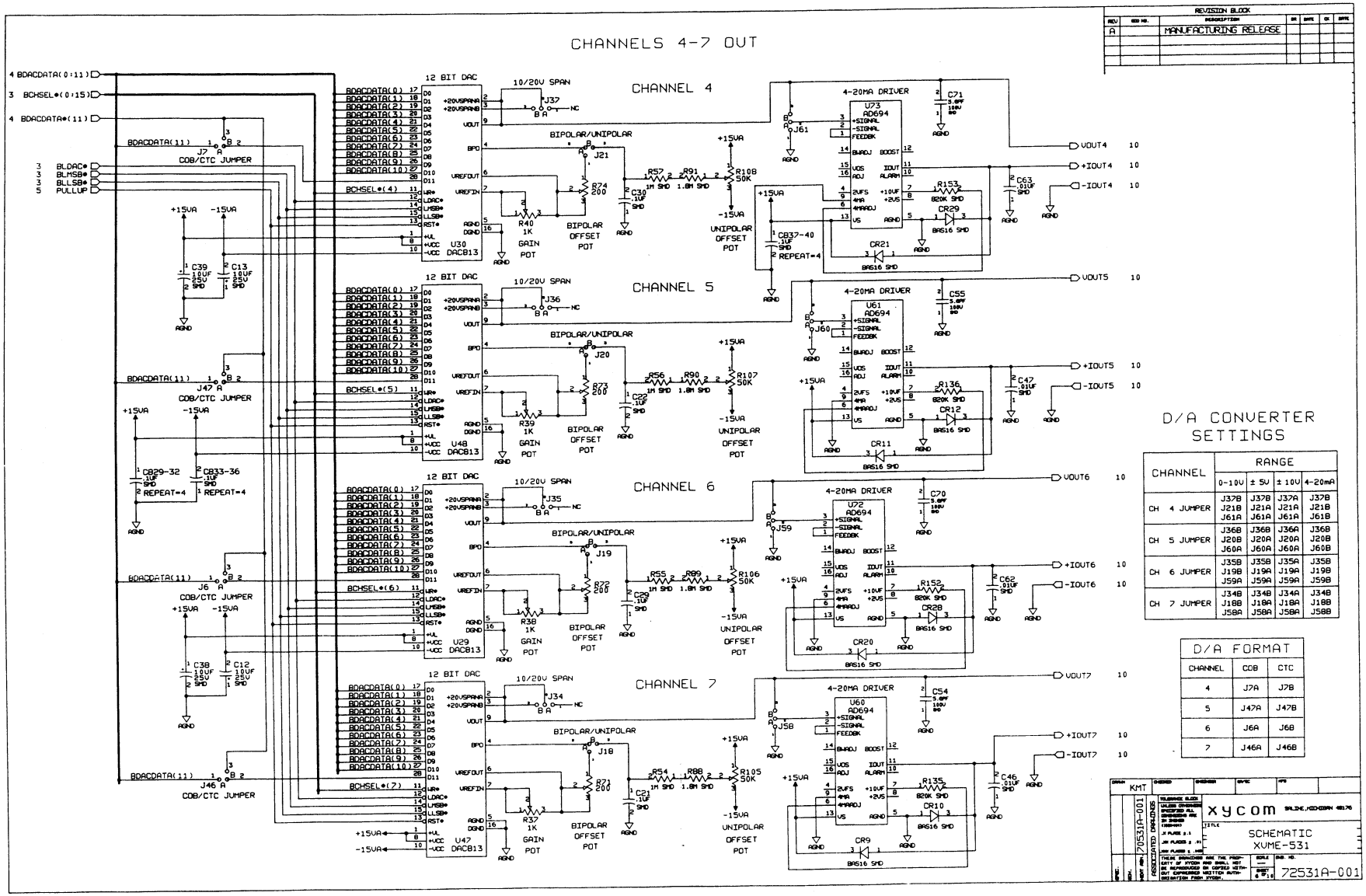
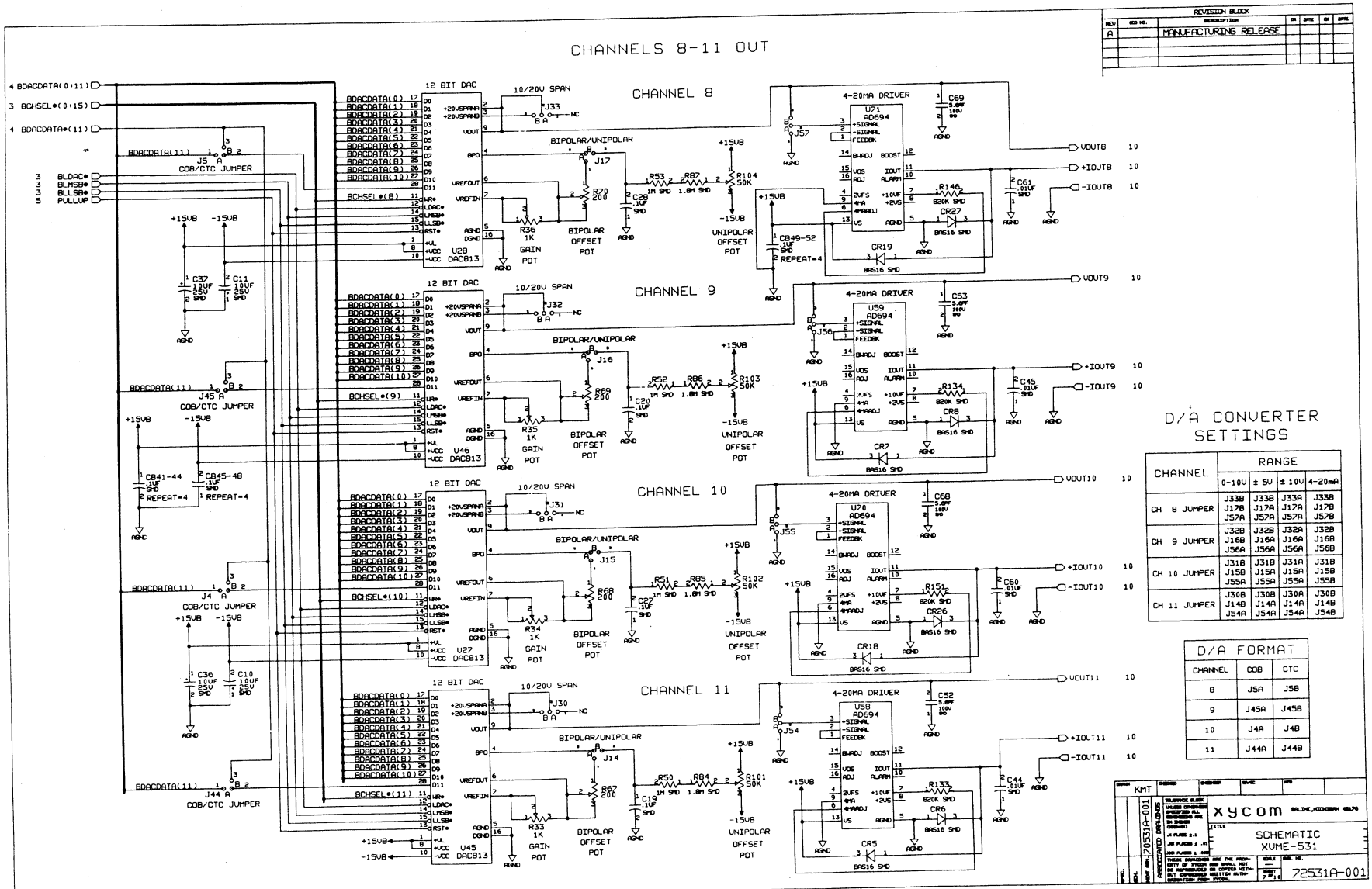

CHANNELS 4-7 OUT
REVISION BLOCK
A MANUFACTURING RELEASE
CHANNEL 4
CHANNEL 5
CHANNEL 6
CHANNEL 7
12 BIT DAC
10/20V SPAN
BIPOLAR/UNIPOLAR
BIPOLAR OFFSET POT
GAIN POT
UNIPOLAR OFFSET POT
4-20MA DRIVER
AD694
COB/CTC JUMPER
REPEAT=4
D/A CONVERTER SETTINGS
CHANNEL
RANGE
0-10V
± 5V
± 10V
4-20mA
CH 4 JUMPER
CH 5 JUMPER
CH 6 JUMPER
CH 7 JUMPER
D/A FORMAT
CHANNEL
COB
CTC
SCHEMATIC
XVME-531
72531A-001

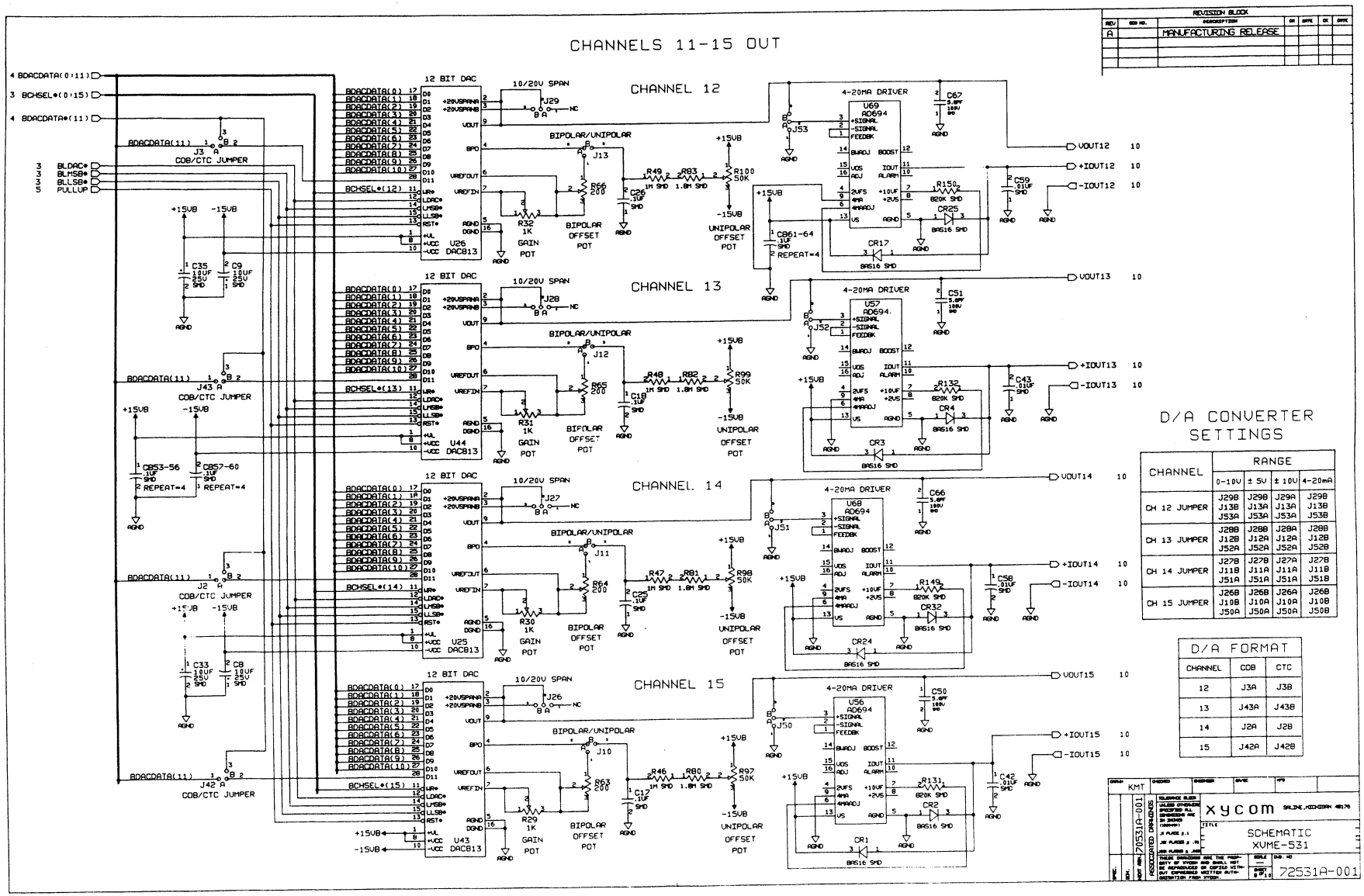


D/A CONVERTER SETTINGS

CHANNEL	RANGE			
	0-10V	± 5V	± 10V	4-20mA
CH 8 JUMPER	J33B J17B J57A	J33B J17A J57A	J33A J17A J57A	J33B J17B J57B
CH 9 JUMPER	J32B J16B J56A	J32B J16A J56A	J32A J16A J56A	J32B J16B J56B
CH 10 JUMPER	J31B J15B J55A	J31B J15A J55A	J31A J15A J55A	J31B J15B J55B
CH 11 JUMPER	J30B J14B J54A	J30B J14A J54A	J30A J14A J54A	J30B J14B J54B

D/A FORMAT

CHANNEL	COB	CTC
8	J5A	J5B
9	J45A	J45B
10	J4A	J4B
11	J44A	J44B



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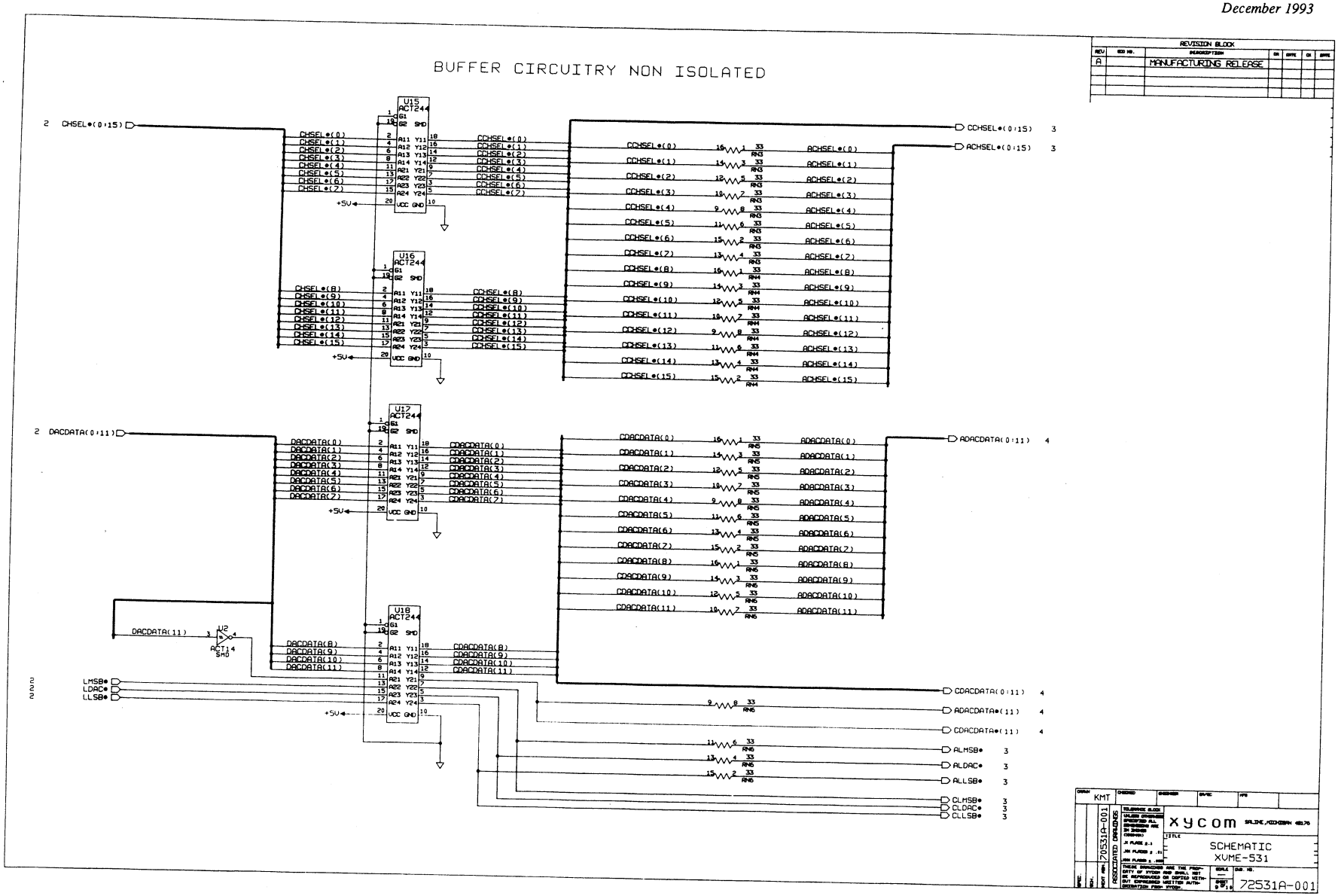
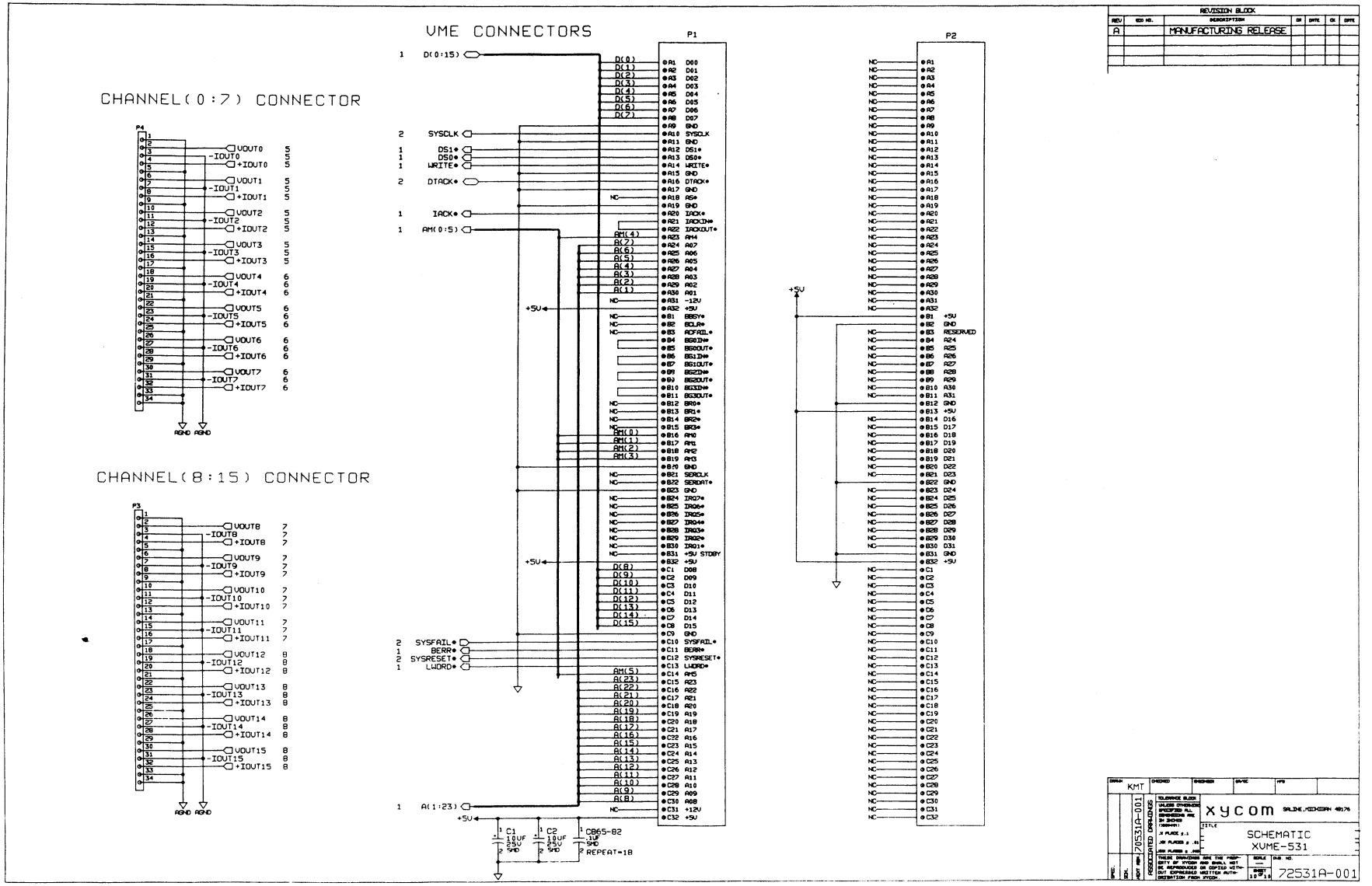

BUFFER CIRCUITRY NON ISOLATED
REVISION BLOCK
REV
DESCRIPTION
MANUFACTURING RELEASE
CHSEL•(0:15)
DACDATA(0:11)
CCHSEL•(0:15)
ACHSEL•(0:15)
ADACDATA(0:11)
CDACDATA(0:11)
ADACDATA•(11)
CDACDATA•(11)
LMSB•
LDAC•
LLSB•
ALMSB•
ALDAC•
ALLSB•
CLMSB•
CLDAC•
CLLSB•
U15 ACT244
U16 ACT244
U17 ACT244
U18 ACT244
U2 ACT14 SMD
+5V
VCC GND
RN3
RN4
RN5
RN6
KMT
xycom
SCHEMATIC
XVME-531
72531A-001


VME CONNECTORS
P1
P2
CHANNEL(0 : 7) CONNECTOR
P4
CHANNEL(8 : 15) CONNECTOR
P3
D(0:15)
SYSCLK
DS1*
DS0*
WRITE*
DTACK*
IACK*
AM(0:5)
A(1:23)
SYSFAIL*
BERR*
SYSRESET*
LWORD*
+5V
AGND
C1 10UF 25V S/MD
C2 10UF 25V S/MD
CB65-82 .1UF S/MD
REPEAT=18
REVISION BLOCK
MANUFACTURING RELEASE
KMT
xycom
SCHEMATIC
XVME-531
72531A-001